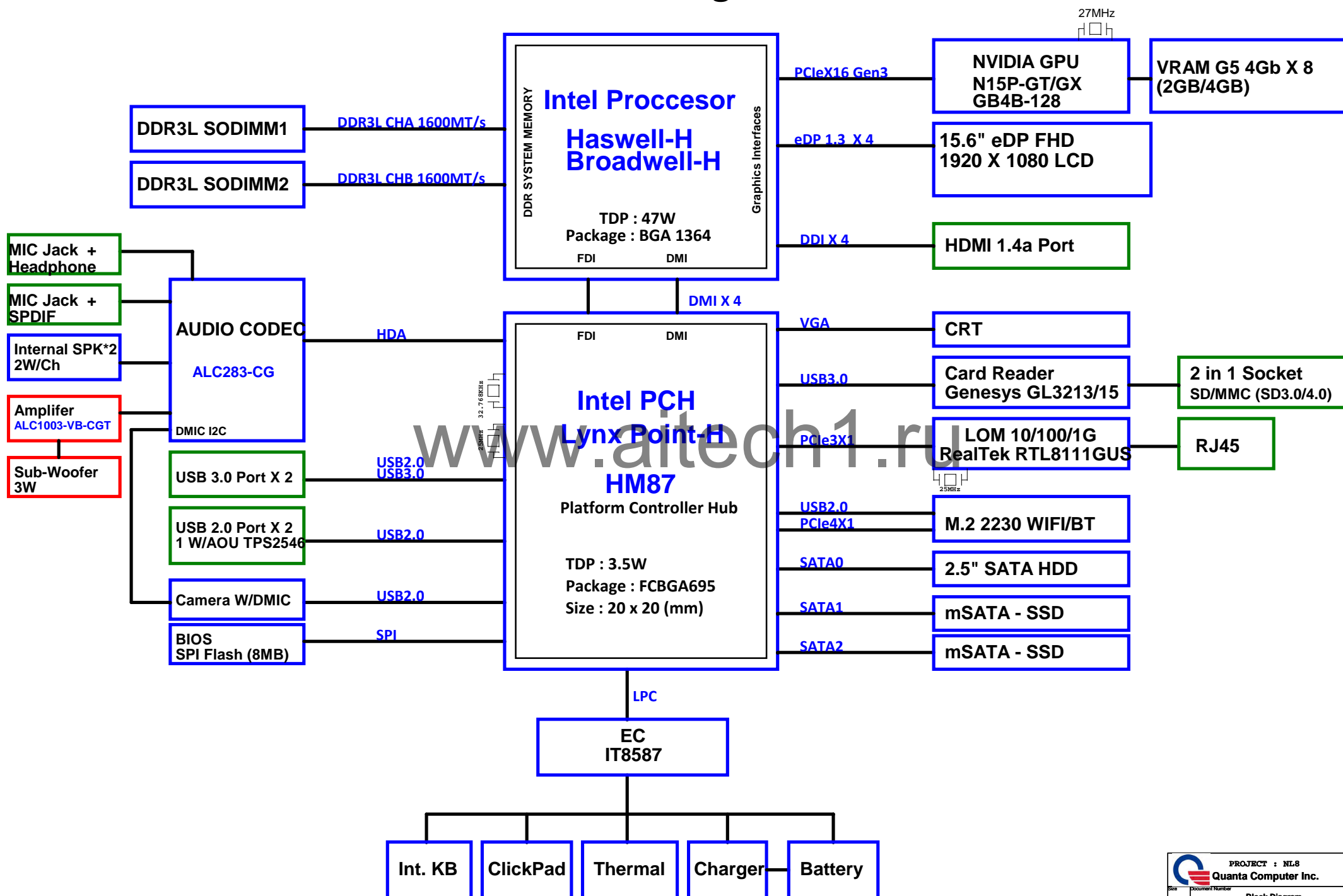
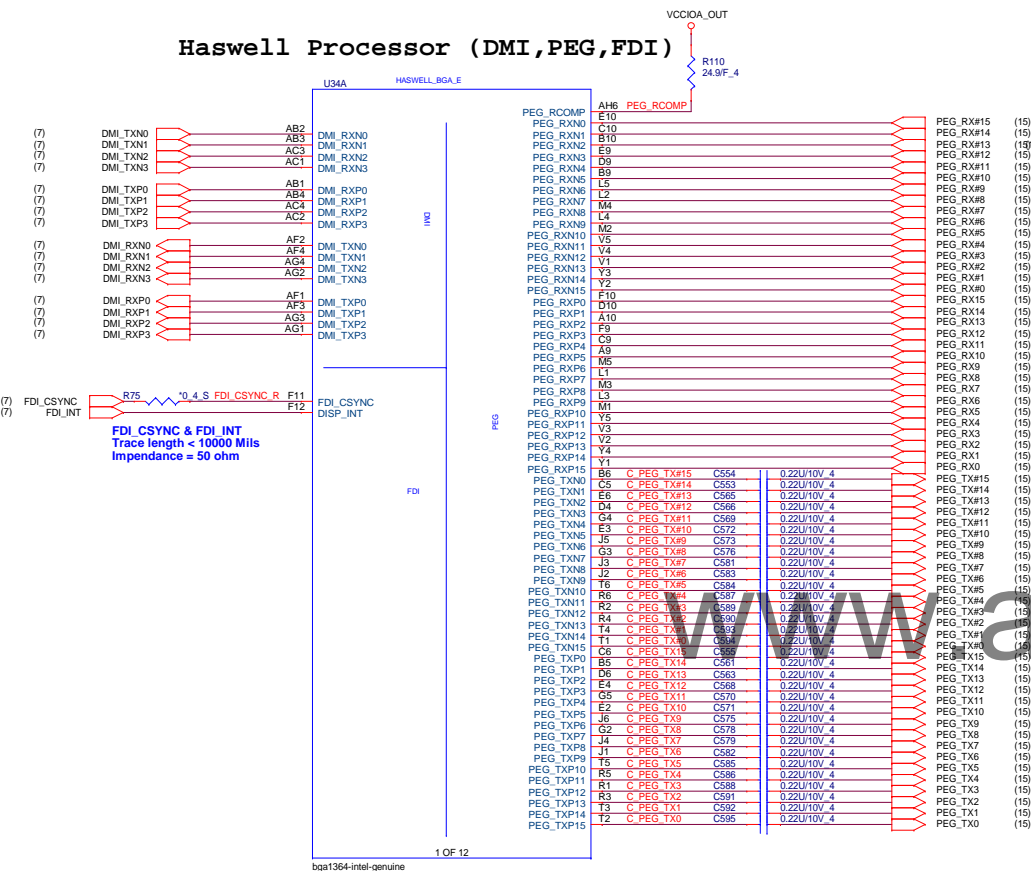


# NL8 Block Diagram

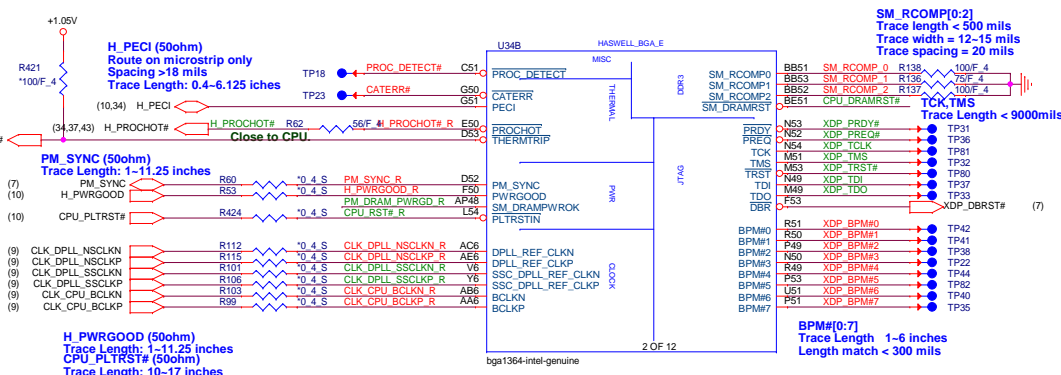


## Haswell Processor (DMI,PEG,FDI)

PEG\_RCOMP  
Trace length < 400 MILS  
Trace width = 12 MILS  
Trace spacing = 15 MILS

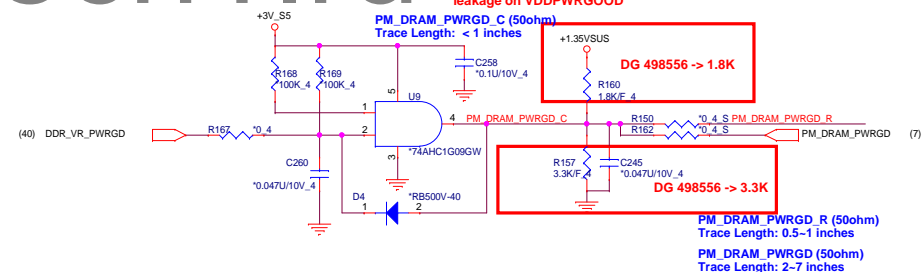


```
Haswell Processor (CLK,MISC,JTAG)
```

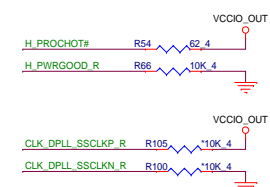


**SM\_DRAMPWROK Processor Input.**

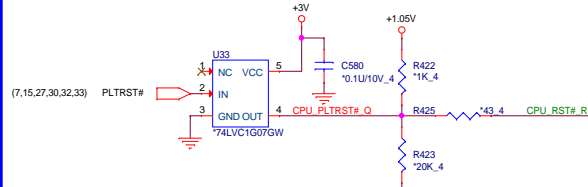
t. To change the resistor values in the DRAMPWROK logic to reduce the leakage on VDDPWROOD



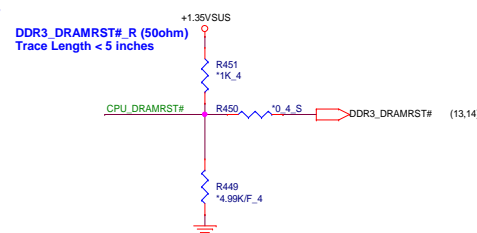
### PU/PD of CPU



## Reserved For buffer reset of PLTRSRIN#



## SM DRAMRST# Topology



## XDP PU/PD





# Haswell Processor (DDI,eDP,FDI)

HDMI

- (24) HDMI\_TX2-
- (24) HDMI\_TX2+
- (24) HDMI\_TX1-
- (24) HDMI\_TX1+
- (24) HDMI\_TX0-
- (24) HDMI\_TX0+
- (24) HDMI\_CLK-
- (24) HDMI\_CLK+

- C25 DDIB\_TXN0
- D25 DDIB\_TXP0
- A25 DDIB\_TXN1
- B25 DDIB\_TXP1
- C24 DDIB\_TXN2
- D24 DDIB\_TXP2
- A24 DDIB\_TXN3
- B24 DDIB\_TXP3

- C21 DDIC\_TXN0
- D21 DDIC\_TXP0
- A21 DDIC\_TXN1
- B21 DDIC\_TXP1
- C20 DDIC\_TXN2
- D20 DDIC\_TXP2
- A20 DDIC\_TXN3
- B20 DDIC\_TXP3

- C16 DDID\_TXN2
- D16 DDID\_TXP2
- A16 DDID\_TXN3
- B16 DDID\_TXP3

- C17 DDID\_TXN0
- D17 DDID\_TXP0
- A17 DDID\_TXN1
- B17 DDID\_TXP1

U34J HASWELL\_BGA\_E

- EDP\_AUXN
- EDP\_AUXP
- EDP\_HPD
- EDP\_TXN0
- EDP\_TXN1
- EDP\_TXP0
- EDP\_TXP1

- EDP\_RCOMP
- EDP\_DISP\_UTIL

- FDI\_TXN0
- FDI\_TXP0
- FDI\_TXN1
- FDI\_TXP1

- F15 EDP\_AUXN (22)
- F14 EDP\_AUXP (22)
- E14 EDP\_HPD\_Q

- C14 EDP\_TXN0 (22)
- A12 EDP\_TXN1 (22)
- D14 EDP\_TXP0 (22)
- B12 EDP\_TXP1 (22)

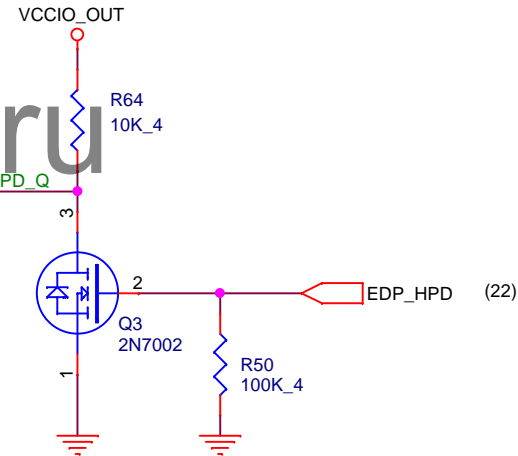
- AG6 EDP\_RCOMP R108 24.9/F 4 VCCIOA\_OUT
- E12

- C12 FDI\_TXN0 (7)
- D12 FDI\_TXP0 (7)
- A14 FDI\_TXN1 (7)
- B14 FDI\_TXP1 (7)

eDP\_RCOMP  
Trace length < 100 mils  
Trace width = 20 mils  
Trace spacing = 25 mils

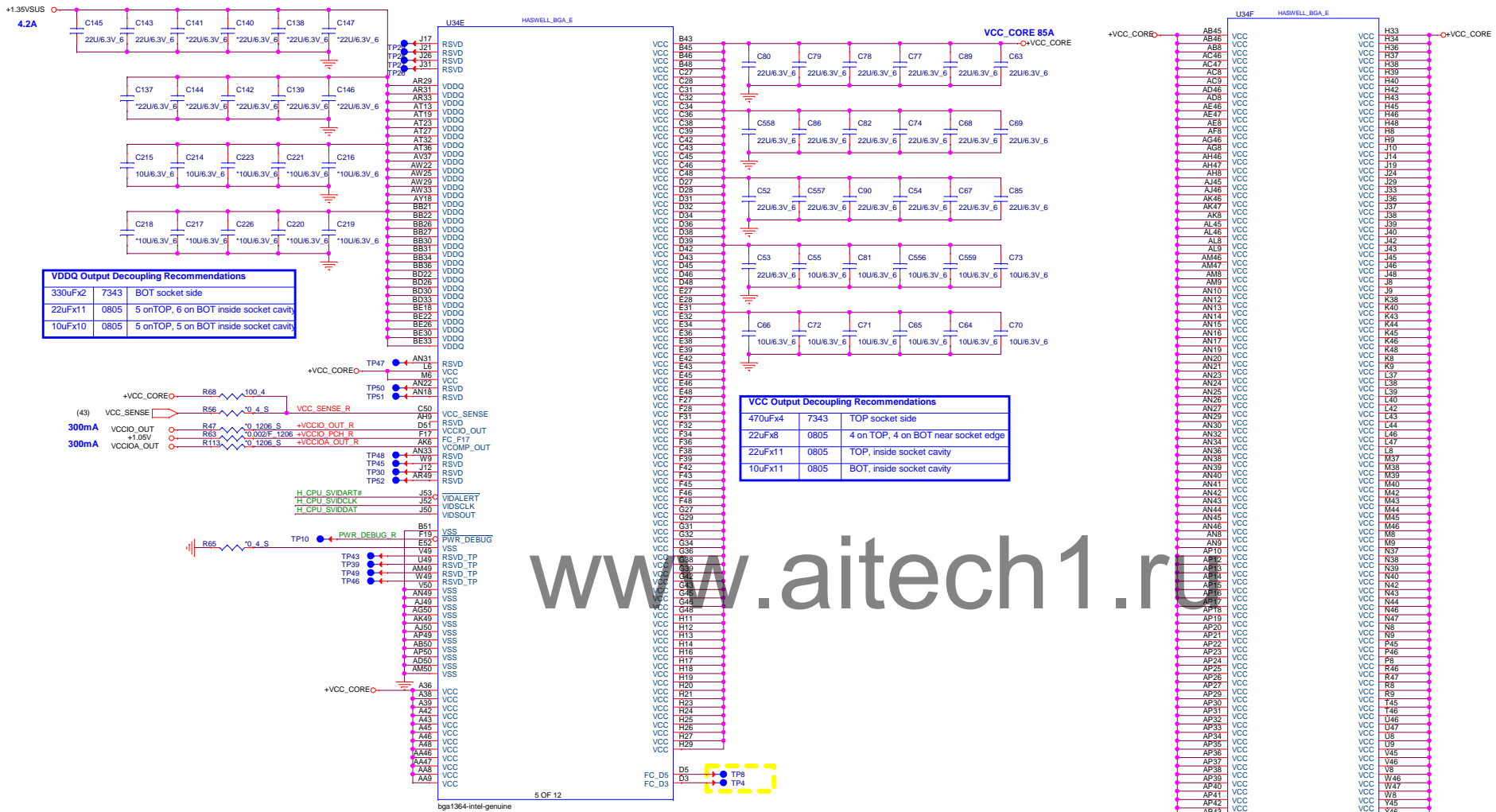
10 OF 12

bga1364-intel-genuine



PROJECT : NL8  
Quanta Computer Inc.

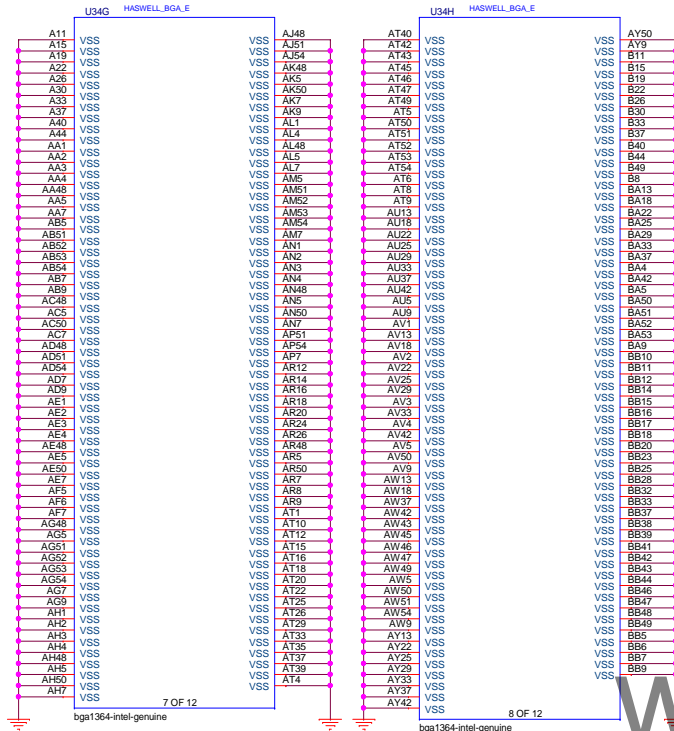




# Haswell Processor (GND)

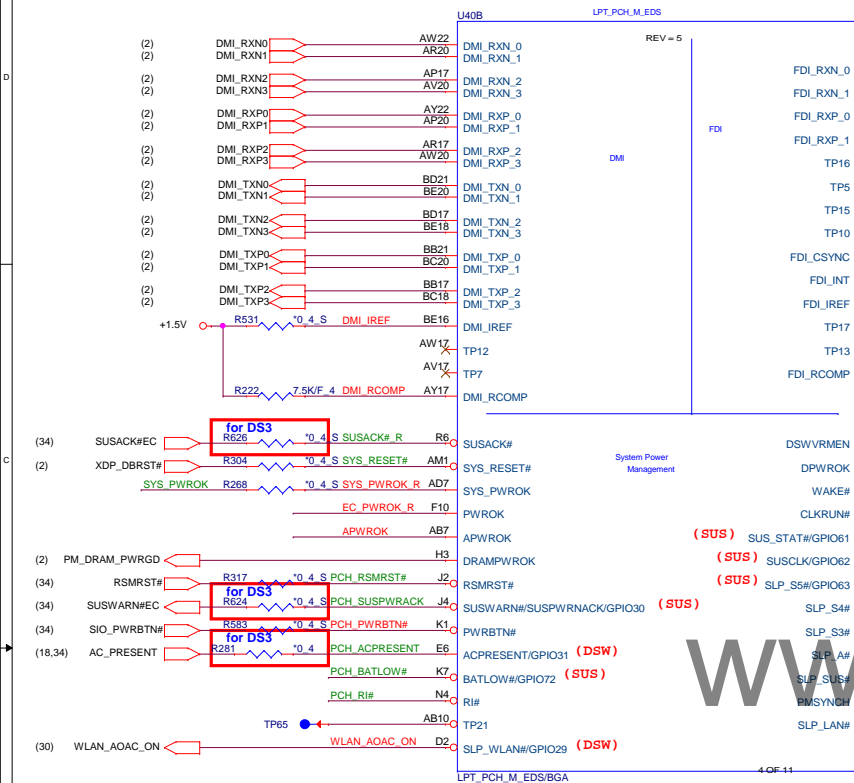
# Haswell Processor (CFG,RSVD)

06

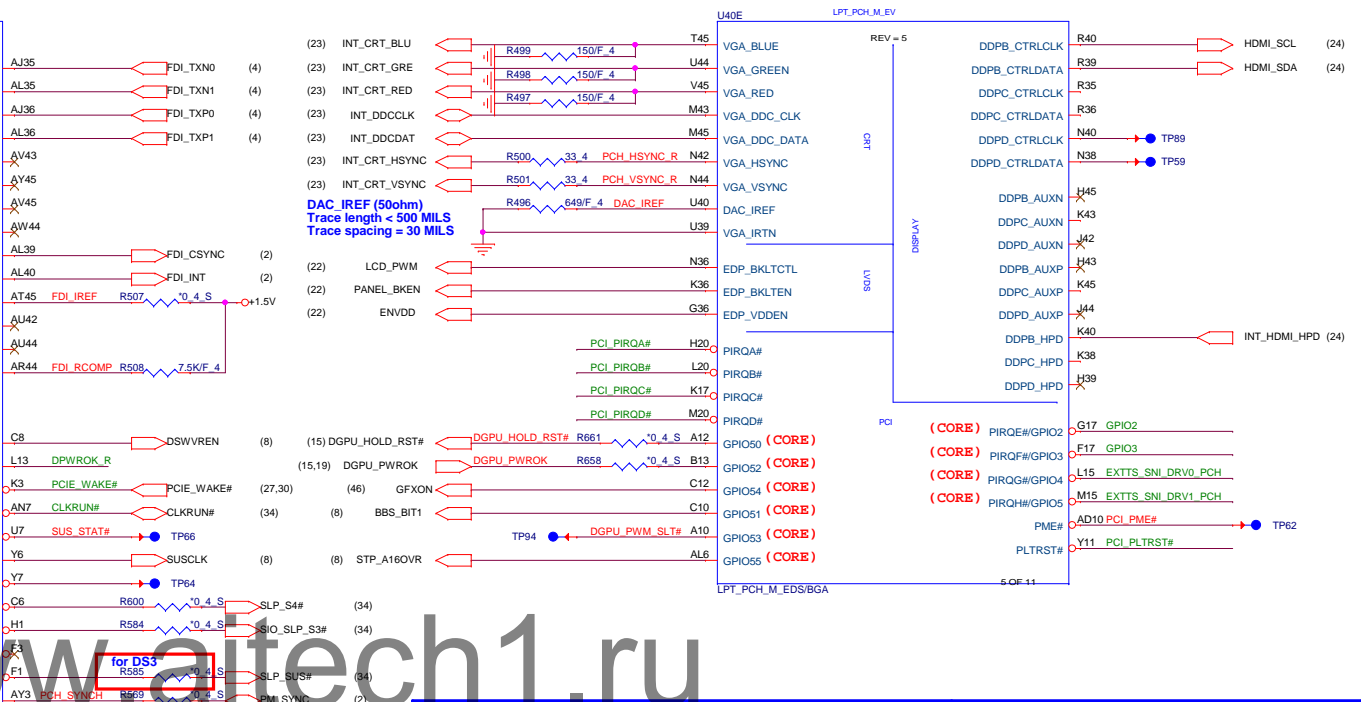


Configuration Signals:		The CFG signals have a default value of '1' if not terminated on the board.	
CFG[2]	PCI Express Static Lane Reversal	x1 = Normal operation x0 = Lane numbers reversed	CFG2 R102 1K 4
CFG[4]	eDP enable	x1 = Disabled x0 = Enabled	CFG4 R95 1K 4
CFG[6:5]	PCI Express Bifurcation	x00 = 1 x8 & 2 x4 PCI Express	CFG6 R91 *1K 4
		x01 = reserved	CFG5 R96 *1K 4
		x10 = 2 x8 PCI Express	
CFG[7]	PEG defer training	x11 = 1 x16 PCI Express	
		x1 = PEG train follow RESETB de-asserted x0 = PEG wait for BIOS fro training	CFG7 R93 *1K 4

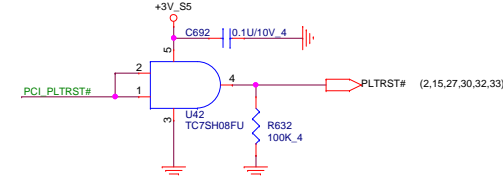
Lynx Point (DMI,FDI,PM)



Lynx Point (CRT,PCI,DDI CNTL)



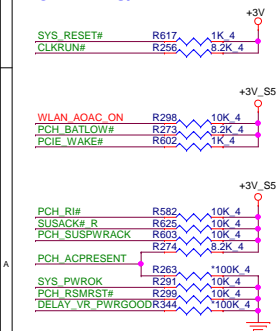
### PLTRST# Buffer



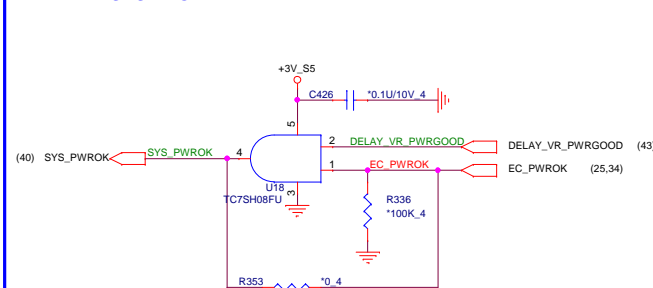
GPIO50  
DGPU\_HOLD\_RST#\_R



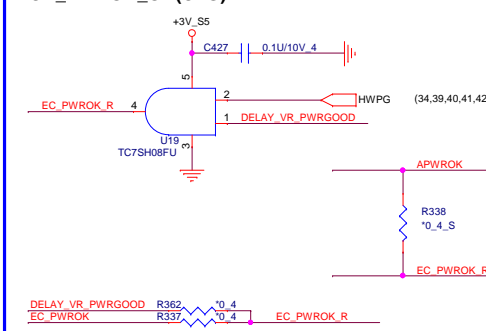
## PCH PM PU/PD



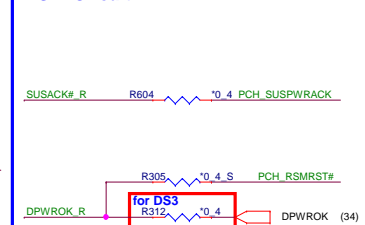
## SYSPWOK



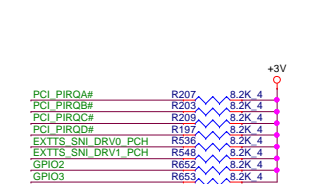
## PCH\_PWROK\_OK(CLG)



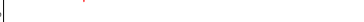
## DSW Circuit



PCI PU



\_\_\_\_\_



\_\_\_\_\_



## (25)



## -ITAG TCK -IT

\_\_\_\_\_



U40A

Page 10

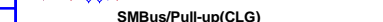
---

U40D LPT\_PCH\_M\_EDS

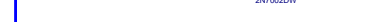
2


$$\frac{PCH\_S}{PCH\_S}$$


## +3V\_S5



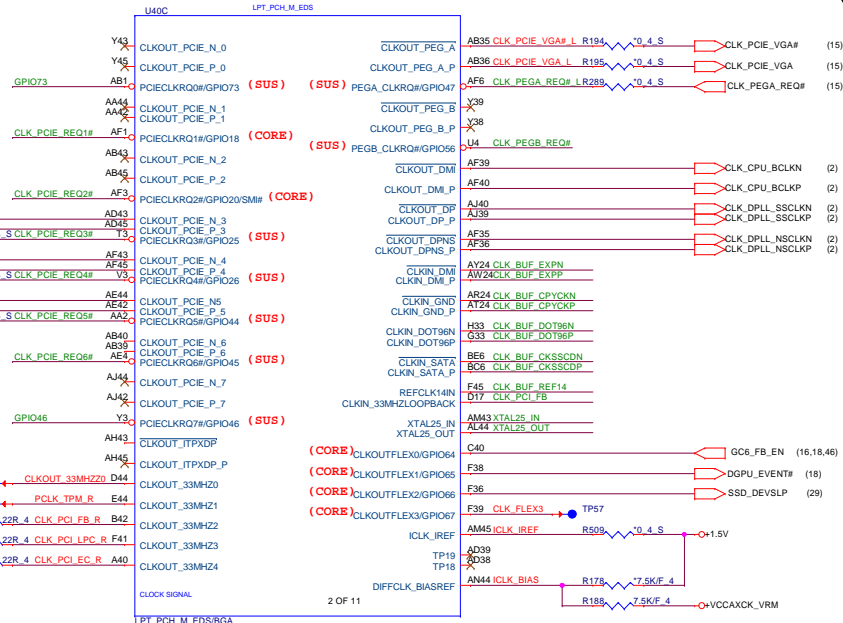
## +3V\_S5



**Lynx Point (PCIe,USB3.0,USB2.0)**



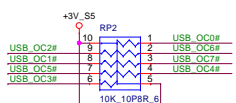
## Lynx Point (CLOCK)



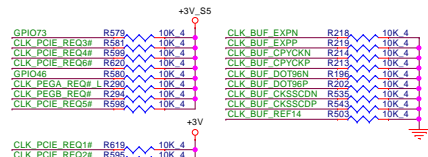
OC Pin	PCH Mapping
OC#0	Port0&1
OC#1	Port2&3
OC#2	Port4&5
OC#3	Port6&7
OC#4	Port8&9
OC#5	Port10&11
OC#6	Port12&13
OC#7	Floater OC#

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## USB Overcurrent

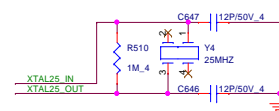


## PCH Internal Clock

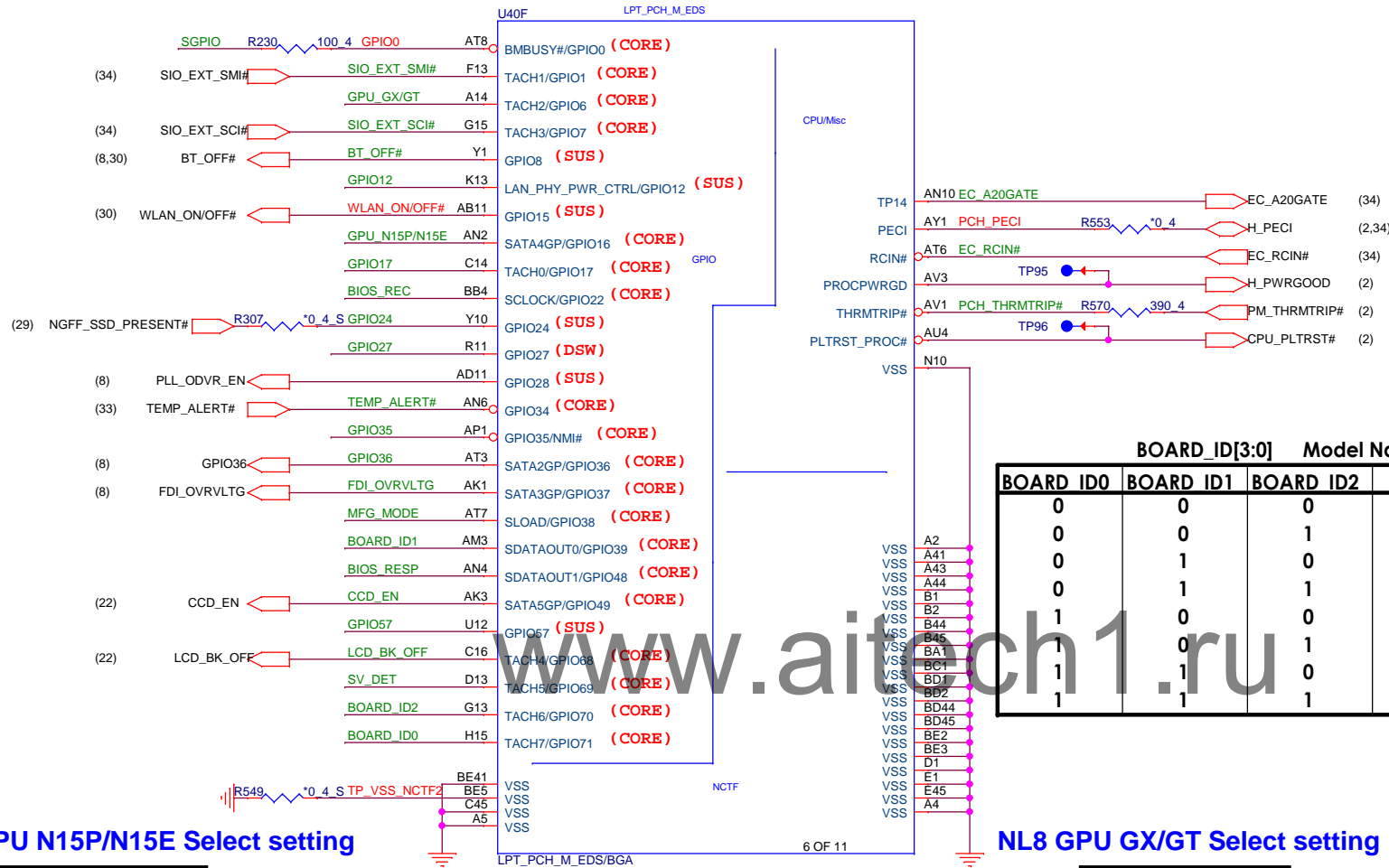


## PCH XDP Signal

Routed by 50 ohm

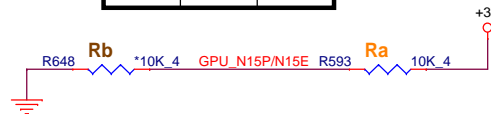


## BOARD ID SETTING



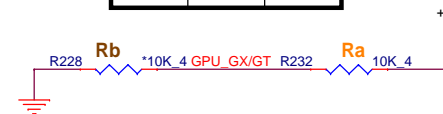
## NL8 GPU N15P/N15E Select setting

GPIO16	N15P	N15E
Stuff	Ra (Hi)	Rb (Lo)

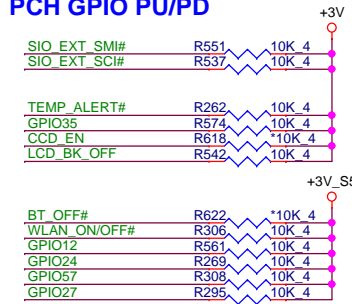


## NL8 GPU GX/GT Select setting

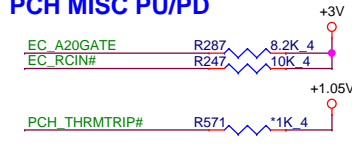
GPIO6	GX	GT
Stuff	Ra (Hi)	Rb (Lo)



## PCH GPIO PU/PD



## PCH MISC PU/PD



## BIOS RECOVERY

0 = Enable  
1 = Disable

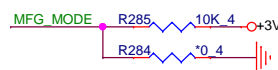


## Swap GPIO

0 = SGPIO  
1 = Default



## MFG TEST



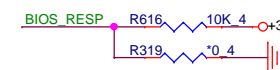
## SV Detect

0 = SV Detect  
1 = Default



## BIOS\_RESP

0 = BIOS RESP  
1 = Default

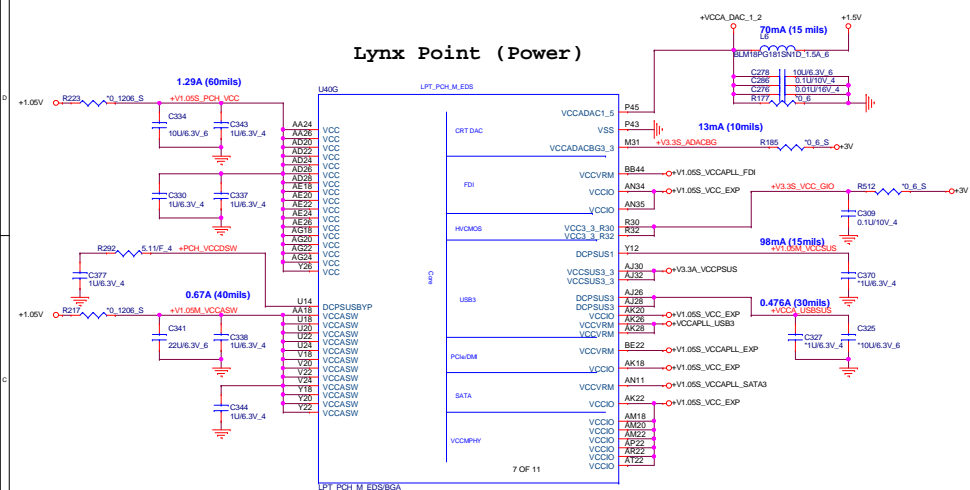


PROJECT : NL8  
Quanta Computer Inc.

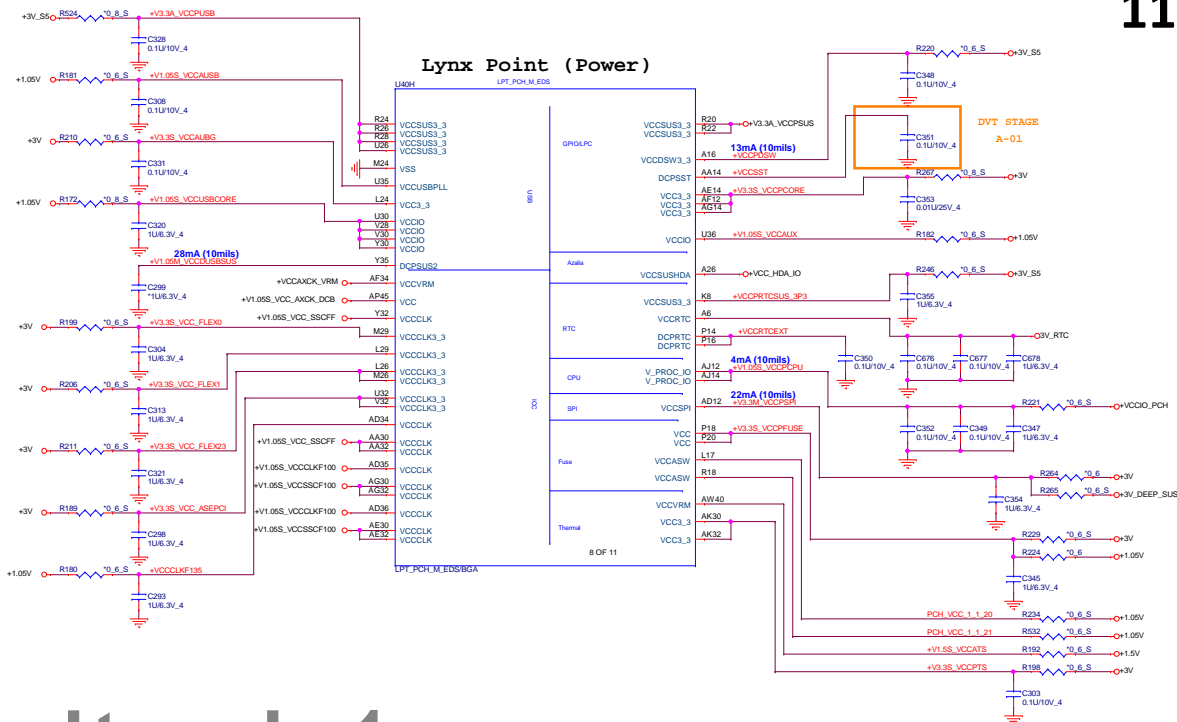
Size	Document Number	Rev
	LPT 4/6 (GPIO/MISC)	1A
Date:	Friday, April 18, 2014	Sheet 10 of 51



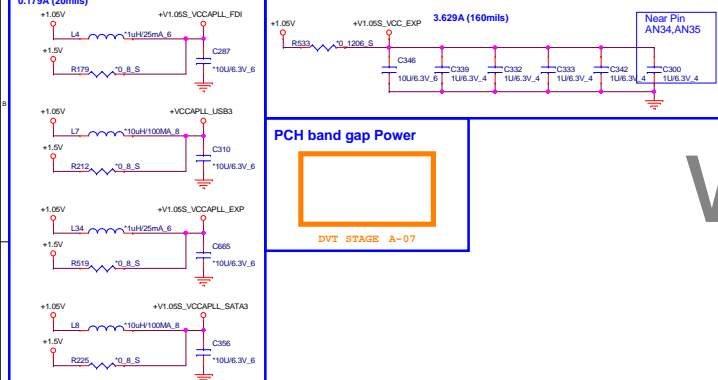
Lynx Point (Power)



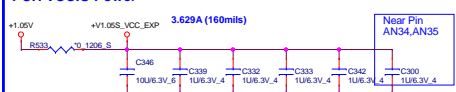
## Lynx Point (Power)



PCH VRM Power	1.05V OPTION IS PROVIDED FOR VALIDATION PURPOSES
0.179A (20mils)	



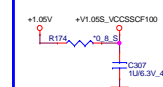
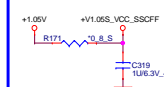
### 3 PCH VCCIO Power



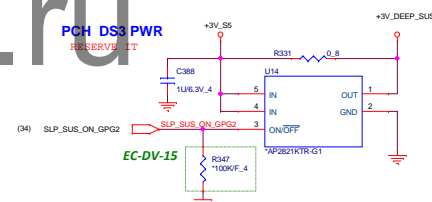
## PCH band gap Power



PCH HDA Power	0.01A (10mils)
---------------	----------------

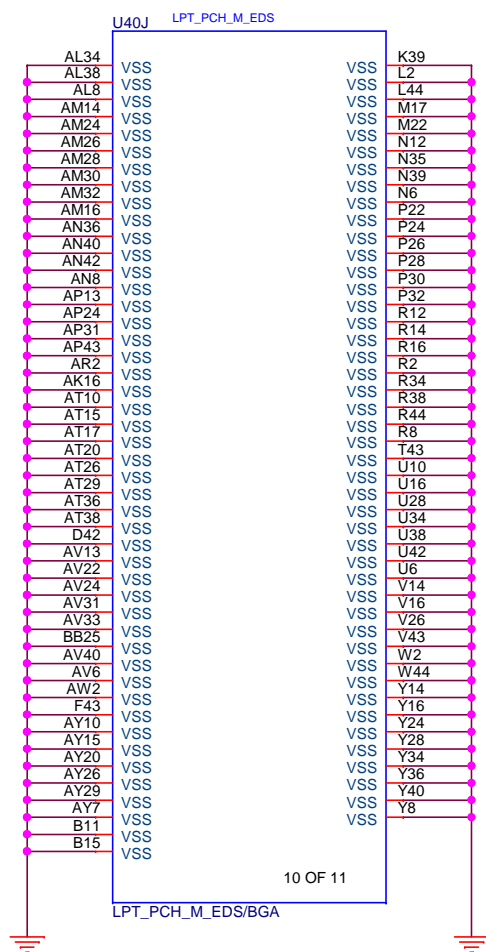


PCH DS3 PWR

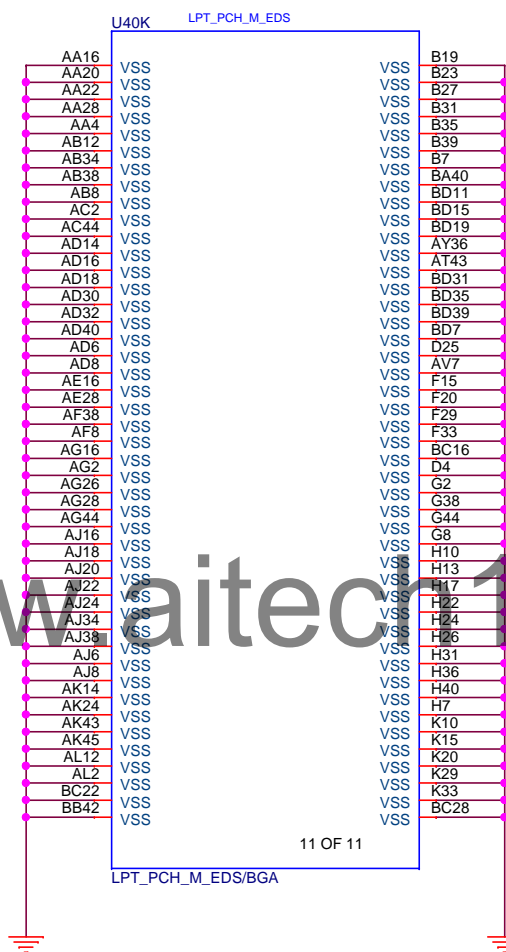




## Lynx Point (GND)



## Lynx Point (GND)





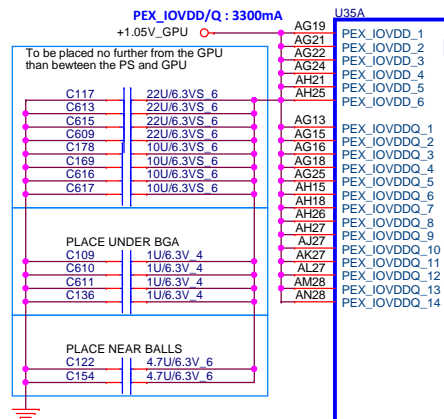
## 3





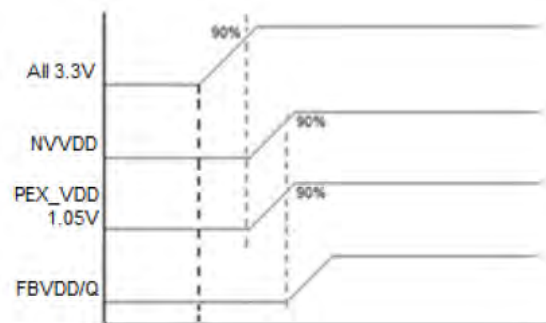
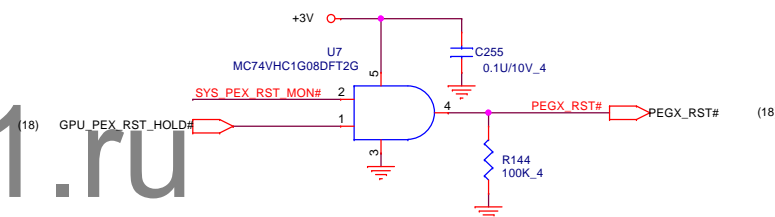
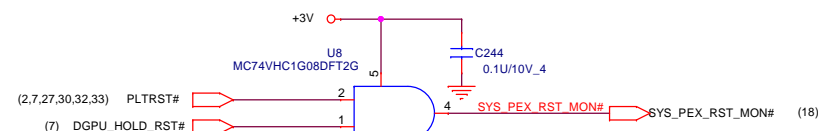
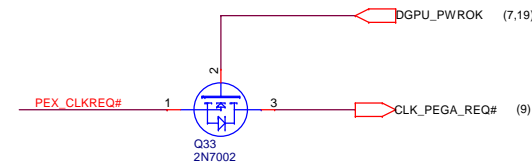
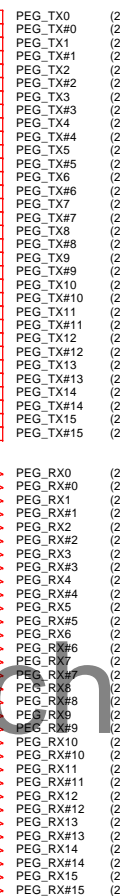
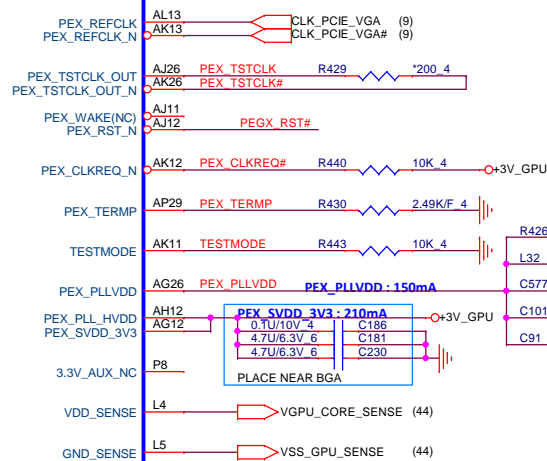
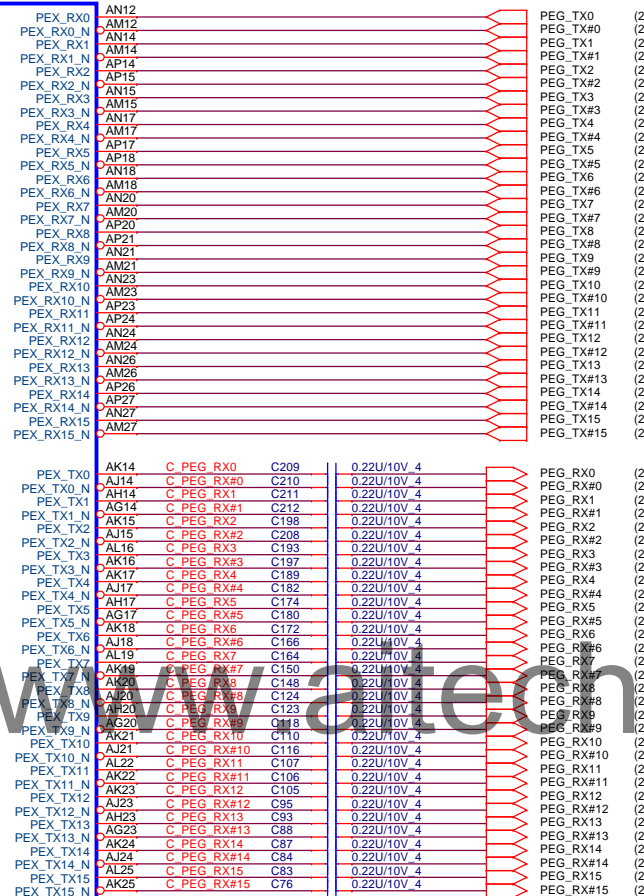
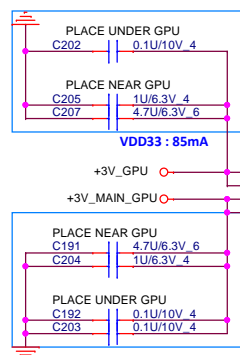
8

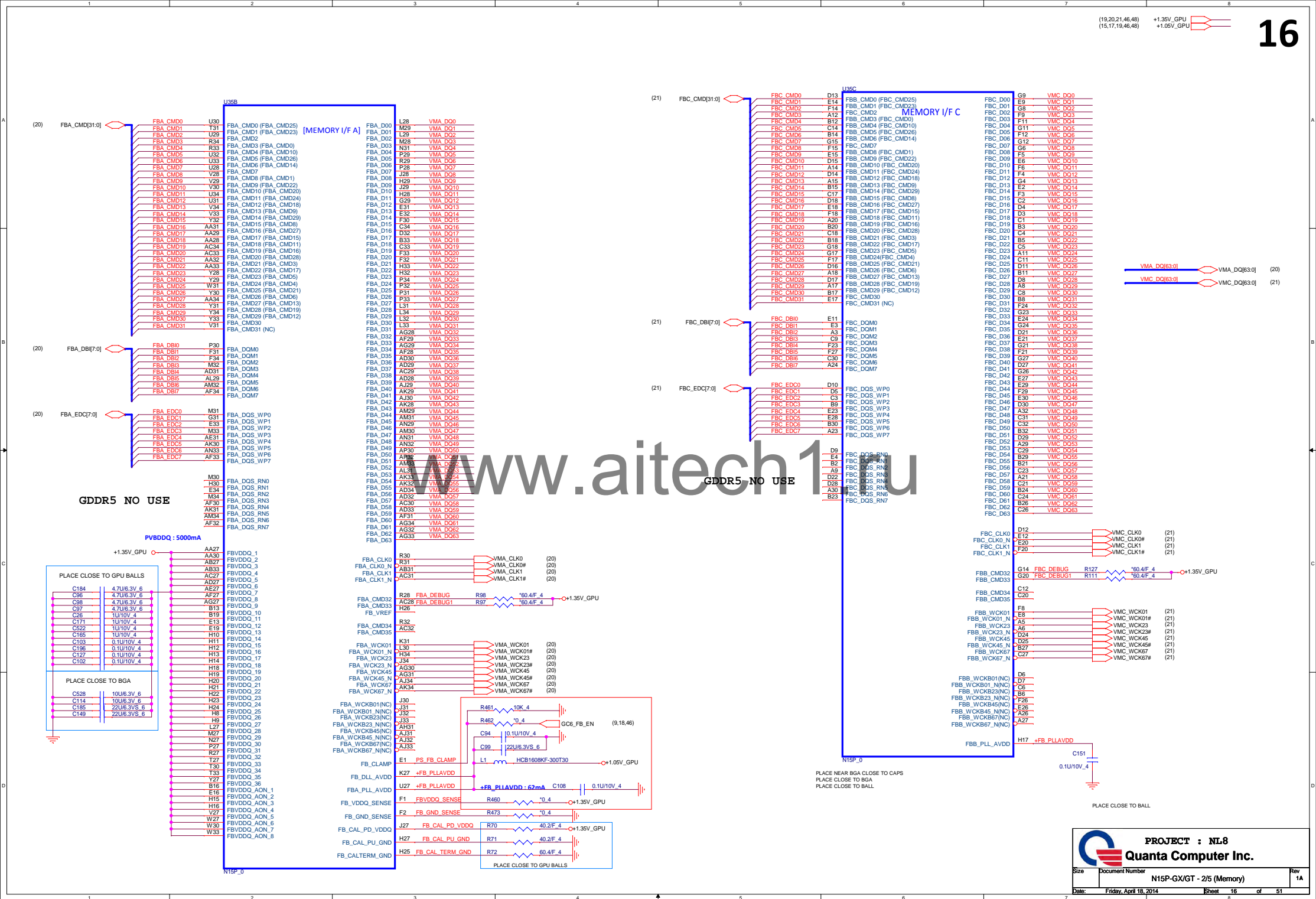


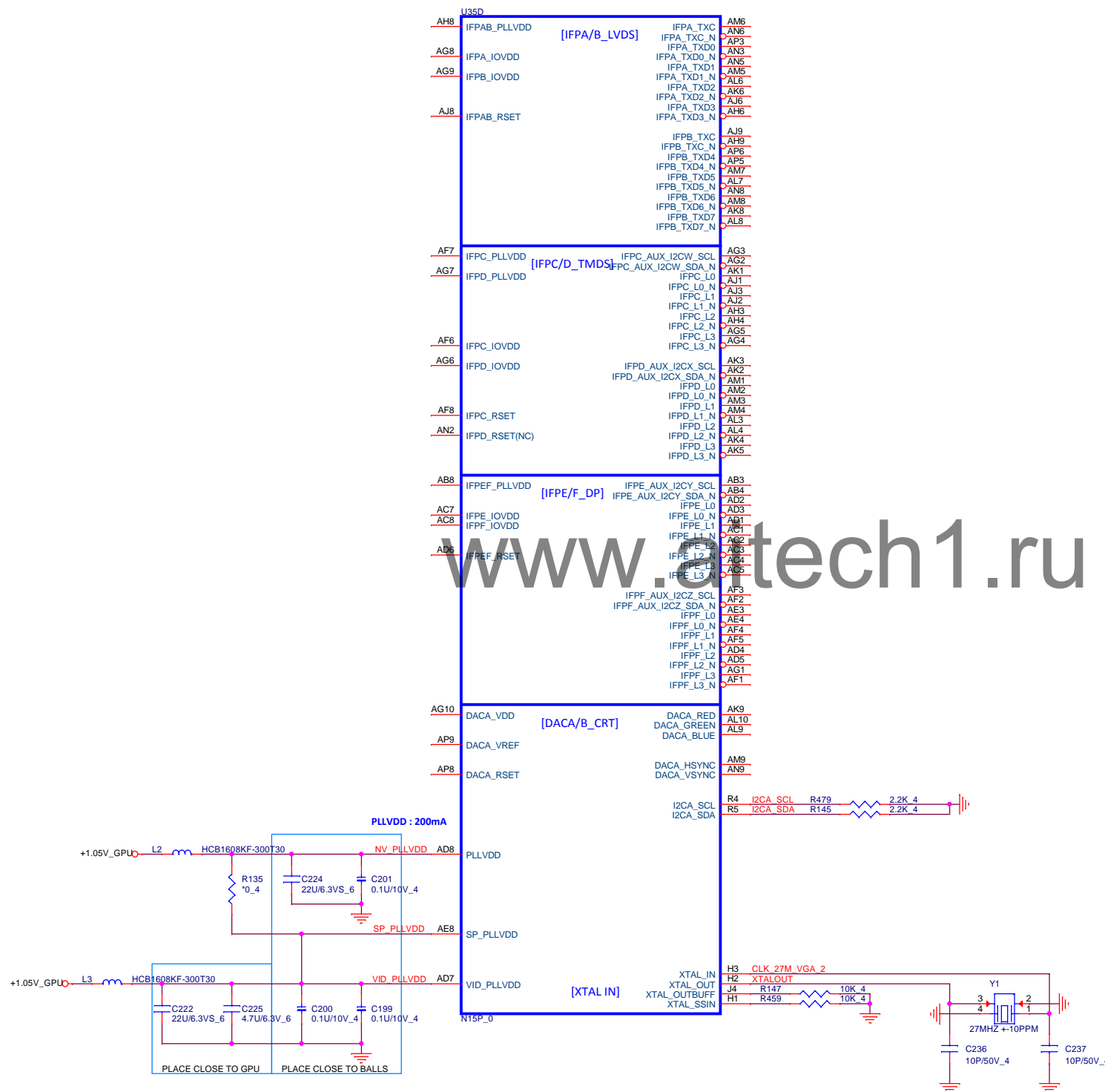


## [PEG Interface]

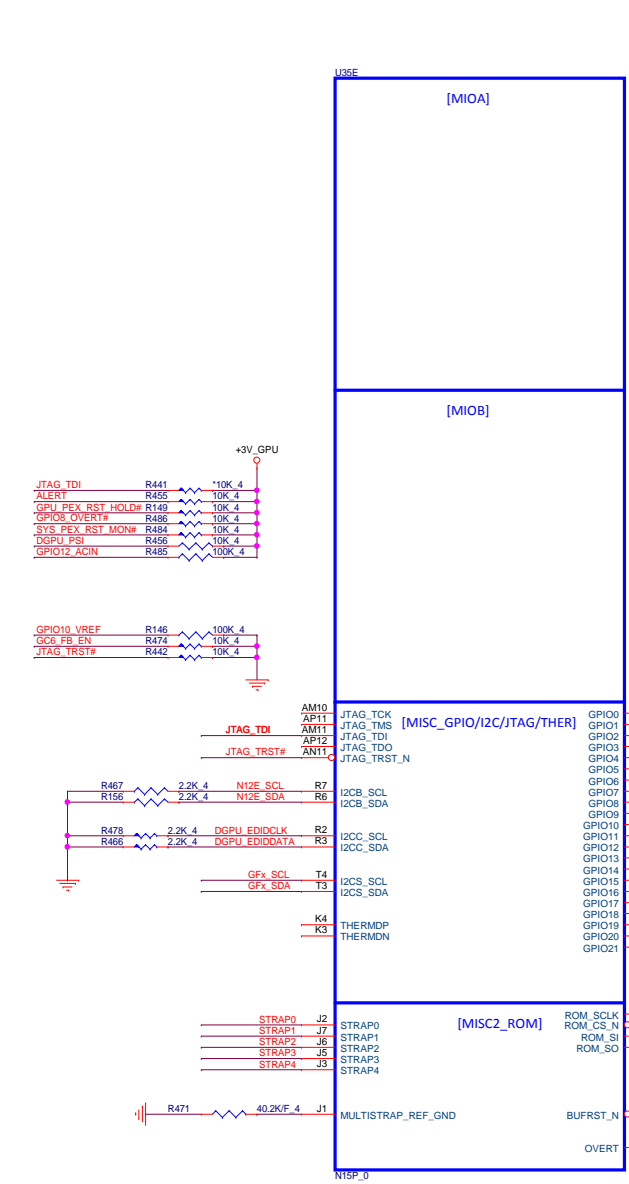
AC8 NC\_1  
AJ28 NC\_2  
AJ4 NC\_3  
AJ5 NC\_4  
AL11 NC\_5  
C15 NC\_6  
D19 NC\_7  
D20 NC\_8  
D23 NC\_9  
D28 NC\_10  
H31 NC\_11  
T8 NC\_12  
V32 NC\_13











Default: GDDR5 Hynix 2G VRAM (for NL8)

Memory Size	Vendor	P/N	Mfr. P/N	ROM_SI	
128M x 16	Hynix (1.35V)	AKG5MWUTW23	H5GC2H24BFR-T2C	0001 (0x1)	10K PD
256M x 16	Hynix (1.35V)	AKG5PWUTW06	H5GC4H24MFR-T2C	0010 (0x2)	15K PD
128M x 16	Samsung (1.35V)	AKG5MWDTS02	K4G20325FD-FC03	0000 (0x0)	4.99K PD
256M x 16	Samsung (1.35V)	AKG5MWDTS05	K4G41325FC-HC03	0011 (0x3)	20K PD

N15P-GX/GT Q8 device ID=0x0FE4

Netname	N14P-GT
ROM_SO	4.99K PU
ROM_SCLK	4.99K PD
STRAP0	49.9K PU
STRAP1	4.99K PD
STRAP2	24.9K PD
STRAP3	4.99K PD
STRAP4	45.3K PD

4.99K/F 4: CS24992FB26 RES CHIP 4.99K 1/16W +1% (0402)  
10K/F 4: CS31002FB26 RES CHIP 10K 1/16W +1% (0402)  
15K/F 4: CS31002FB24 RES CHIP 15K 1/16W +1% (0402)  
20K/F 4: CS32002FB29 RES CHIP 20K 1/16W +1% (0402)  
24.9K/F 4: CS32492FB16 RES CHIP 24.9K 1/16W +1% (0402)  
30.1K/F 4: CS33012FB18 RES CHIP 30.1K 1/16W +1% (0402)  
34.8K/F 4: CS33482FB22 RES CHIP 34.8K 1/16W +1% (0402)  
45.3K/F 4: CS34532FB18 RES CHIP 45.3K 1/16W +1% (0402)  
Logical Strap Bit Mapping

Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99 k	1000	0000
10.0 k	1001	0001
15.0 k	1010	0010
20.0 k	1011	0011
24.9 k	1100	0100
30.1 k	1101	0101
34.8 k	1110	0110
45.3 k	1111	0111

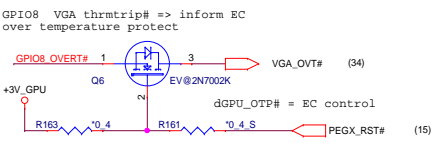
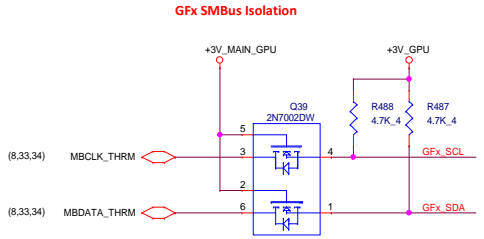
Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	PCL_DEV0[4]	SUB_VENDOR	PCL_DEV0[5]	PEX_PLL_EN_TERM
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	PCL_DEV0[3]	PCL_DEV0[2]	PCL_DEV0[1]	PCL_DEV0[0]
STRAP3	SOR2_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	PCIE_SPEED_CHANG	PCIE_SPEED_CHANG	PCIE_MAX_SPEED	DP_PLL_VDDIOV

Table 9. H14P-GV/GT/GS/LP/GE GDDR5 Recommended Memories 128Mx16 Configuration

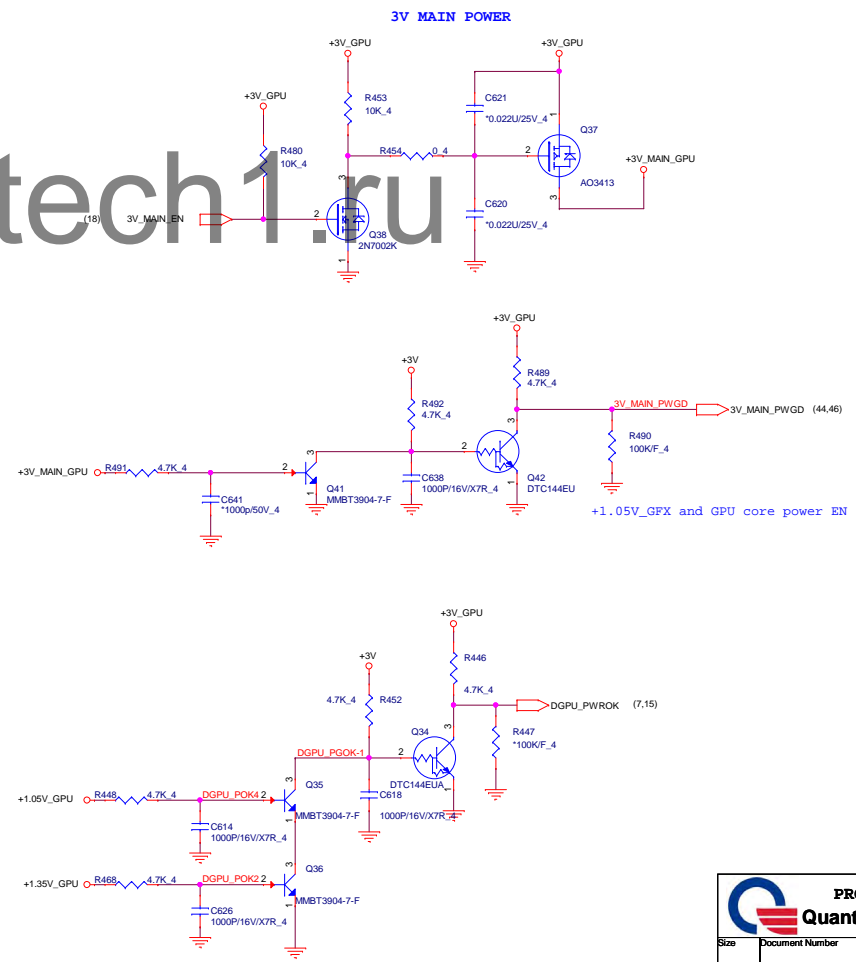
Configuration	Vendor	Strap	FBVDDQ / FBVDDQ	Manufacturer Part Number	Max Speed WCL (MHz)	Memory Data Code Minimum	Status
128Mx16 GDDR5	Hynix	Strap0	1.5 V / 1.5 V	H5GQ2H24BFR-T2C	2300	N/A	Production Candidate
		Strap1	1.5 V / 1.5 V	H5GQ2H24BFR-T2C	2000	N/A	Production Candidate
	Samsung	Strap5	1.5 V / 1.5 V	K4G20325FD-FC04	2500	1219	Production Candidate
		Strap7	1.5 V / 1.35 V	K4G20325FD-FC04	2000	1219	Production Candidate

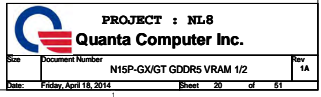
GPIO ASSIGNMENTS

GPIO	Function
GPIO 0	Debug Service Header
GPIO 1	MEM_VDD_CTL/FAN_PWM
GPIO 2	LCD Brightness Control (BL_PWM)
GPIO 3	LCD Power Enable (PPEN)
GPIO 4	LCD Backlight Enable (BLEN)
GPIO 5	NVDD PWM_VID_BOOT_EN
GPIO 6	Remote Sensor Error Correction
GPIO 7	3D STEREO
GPIO 8	GPU Overtemp
GPIO 9	GPU Thermal Alert/FAN_PWM
GPIO 10	FB Vref Control
GPIO 11	NVDD PWM_VID
GPIO 12	PWR_Level AC Detect
GPIO 13	NVDD PSI
GPIO 14	FB_CLAMP_TGL_REG/HPD for IFP AB (not used)
GPIO 15	HPD for IFP C (DP)
GPIO 16	Fan PWM/MEM_VDD_CTL/NVDD PSI/FAN LOCK
GPIO 17	HPD for IFP D (eDP)
GPIO 18	HPD for IFP E (DP)
GPIO 19	HPD for IFP F (DP)
GPIO 20	<not used>
GPIO 21	<not used>



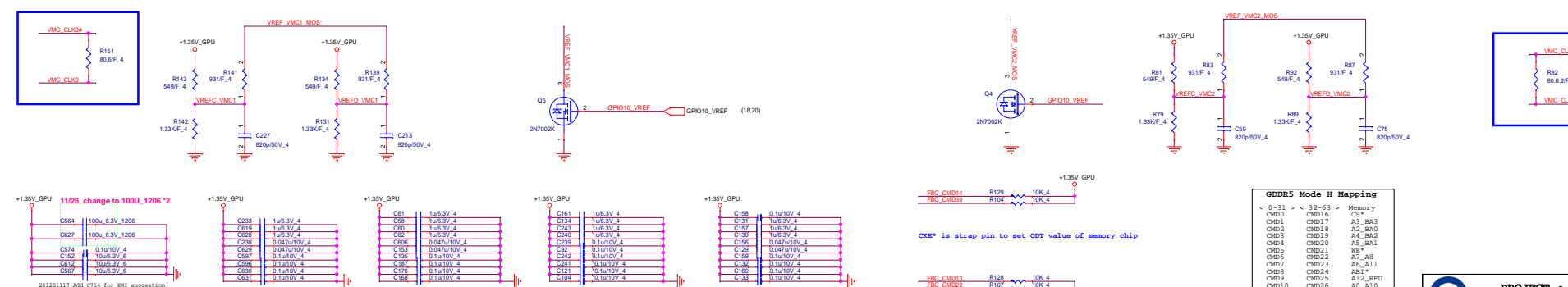






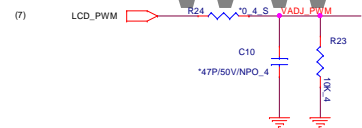
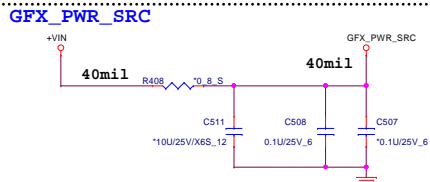
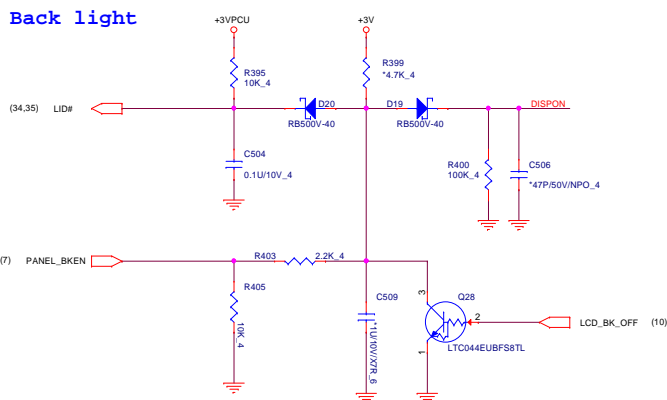
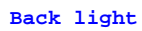
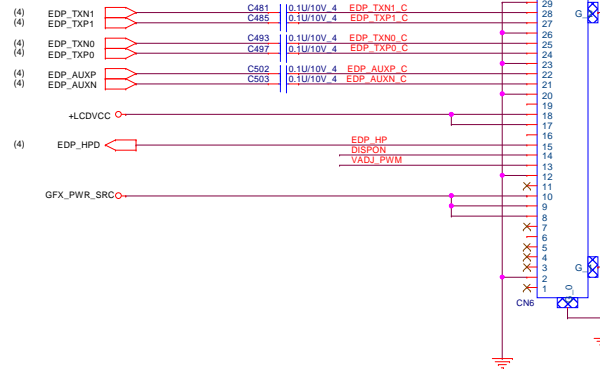
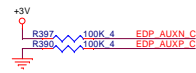
Channel 1  
<32-63>

MF=1 Mirrored



A circuit diagram of a transmission line. A horizontal line represents the transmission line, with a red arrow pointing to the right indicating the direction of signal flow. The line is terminated at the right end by a resistor, represented by a blue zigzag symbol. The resistor is connected to a ground symbol, which consists of three horizontal lines of decreasing width. The text "RGM PD plane @ the end of driver chain" is written below the diagram.

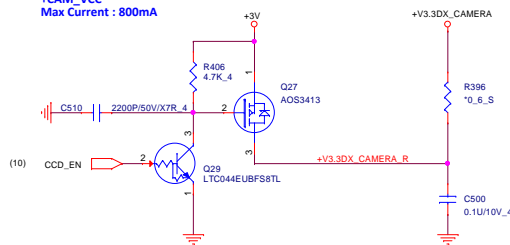
GDDR5 Mode H Mapping		
< 0-31 >	< 32-63 >	Memory
CMD0	CMD16	CS*
CMD1	CMD17	A3_BA0
CMD2	CMD18	A2_BA3
CMD3	CMD19	A4_BA2
CMD4	CMD20	A5_BA1
CMD5	CMD21	WE*
CMD6	CMD22	A7_A8
CMD7	CMD23	A6_A11
CMD8	CMD24	AB1*
CMD9	CMD25	A12_RFU
CMD10	CMD26	A0_A10
CMD11	CMD27	A1_A9
CMD12	CMD28	RAS*
CMD13	CMD29	RST*
CMD14	CMD30	CKE*
CMD15	CMD31	CS*



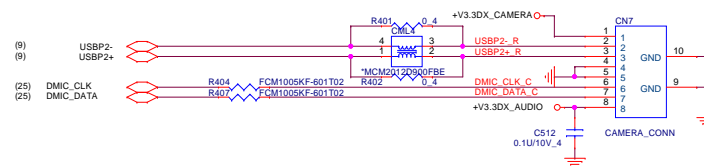
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## CAMERA VCC Control

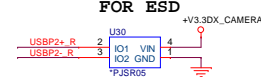
+CAM\_VCC  
Max Current : 800mA

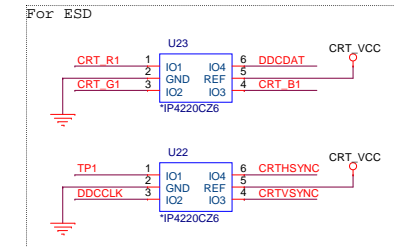
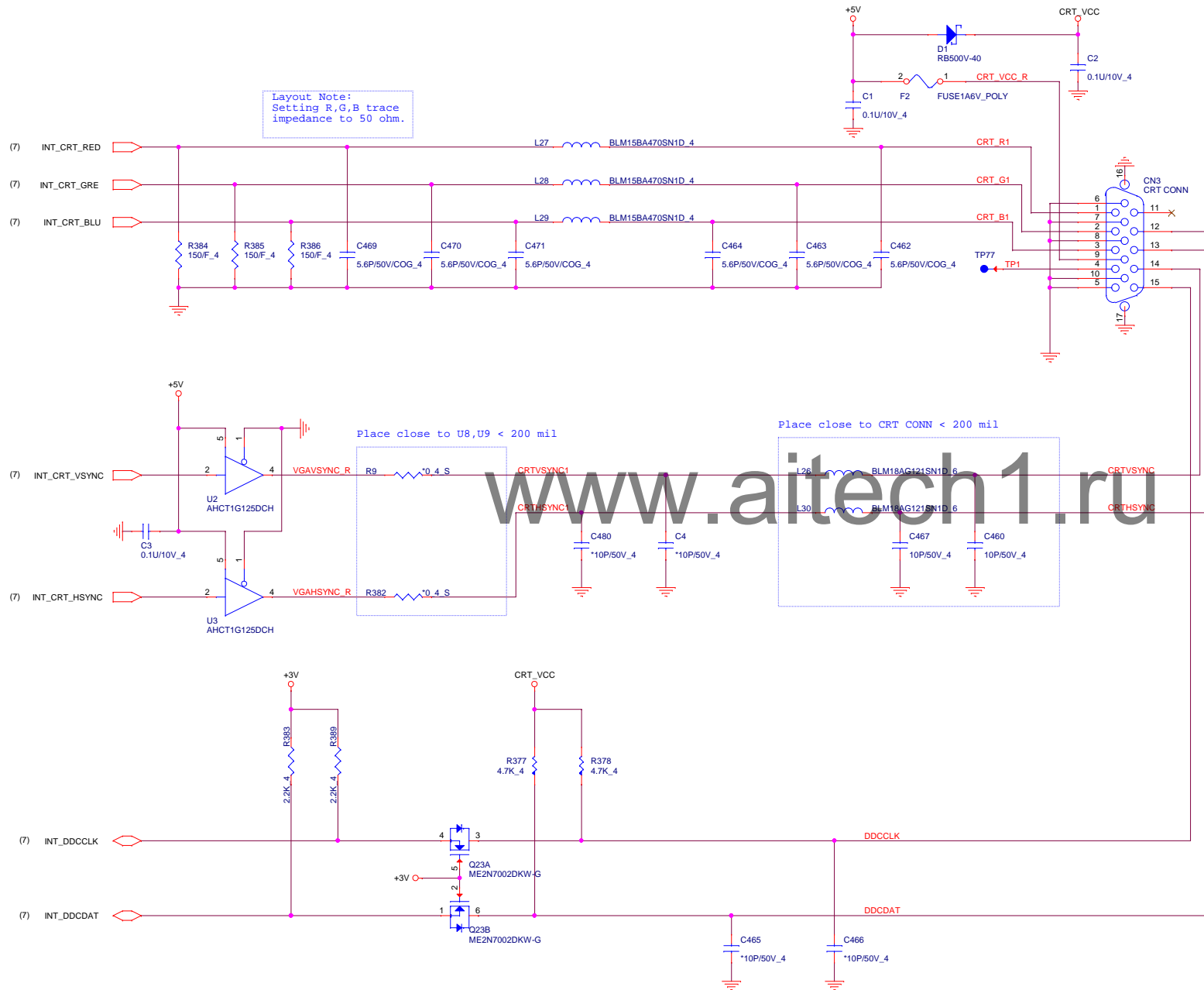
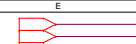


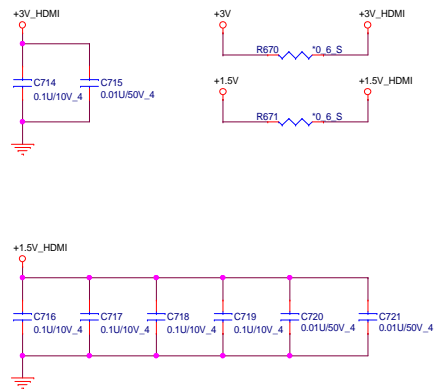
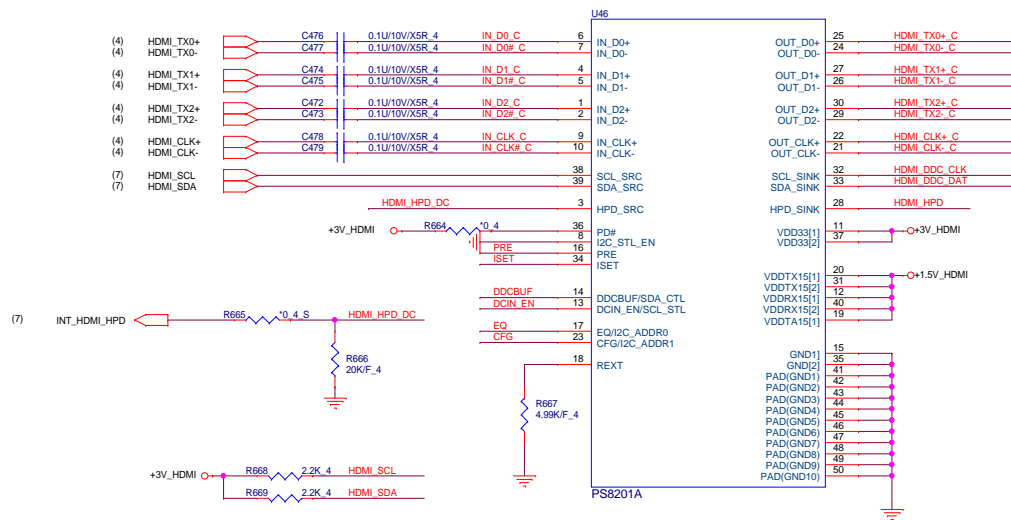
## CAMERA/DMIC CONN



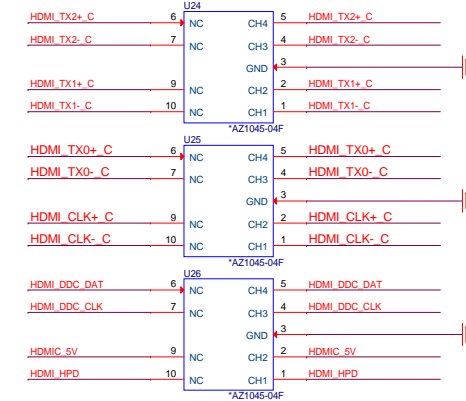
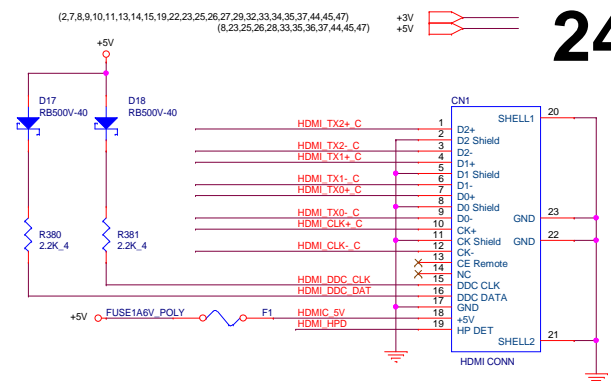
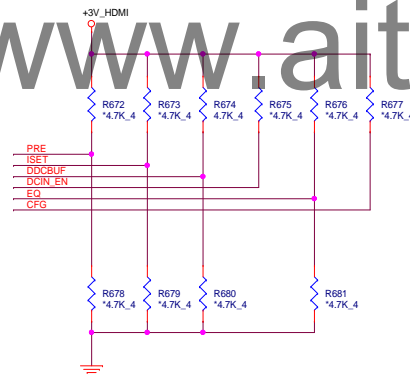
FOR ESD





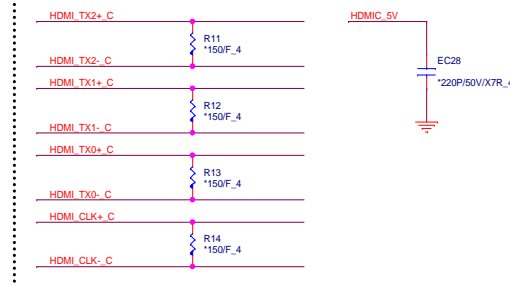


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For ESD Layout note: Place close to HDMI Conn

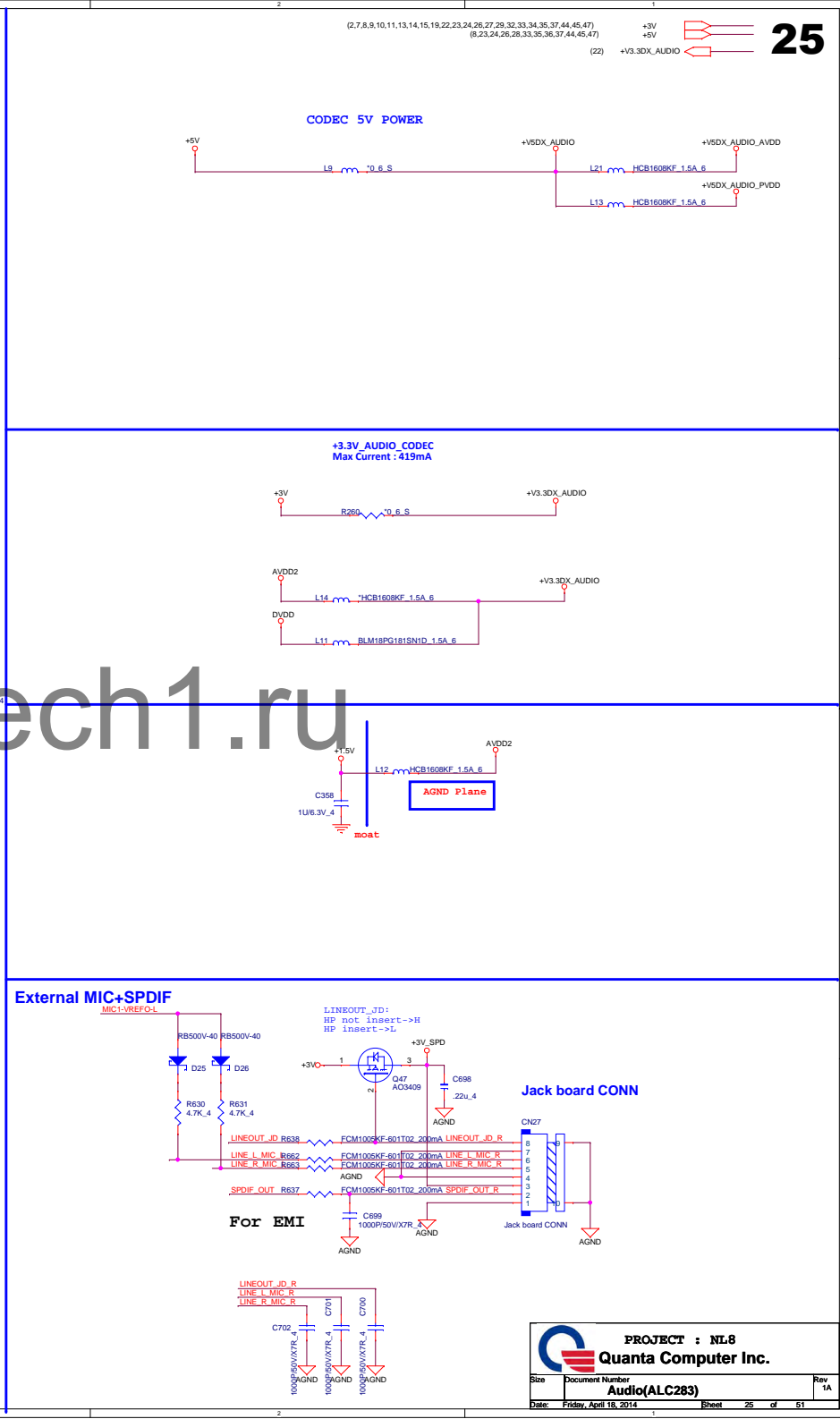
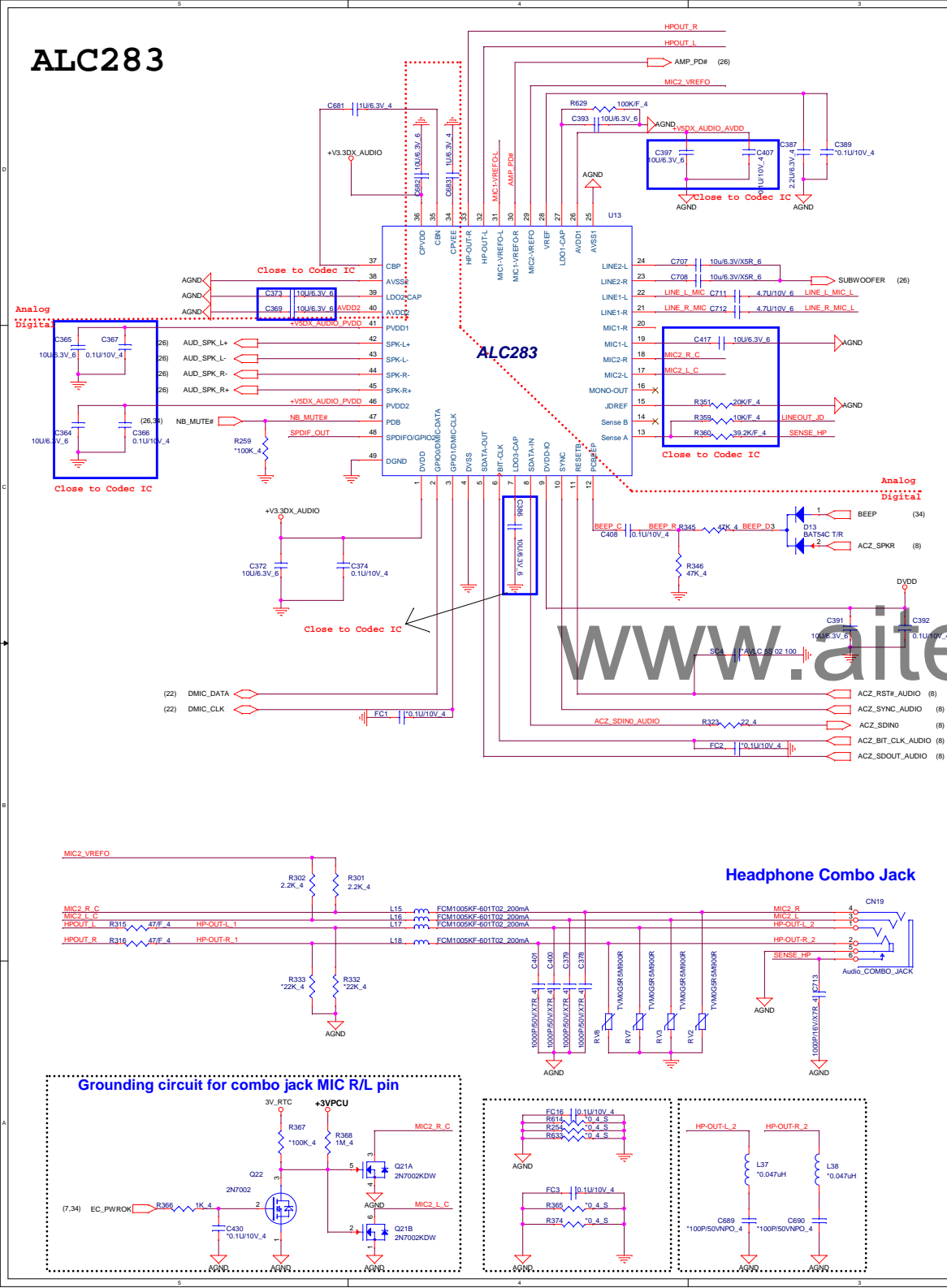
### EMI reserve for HDMI



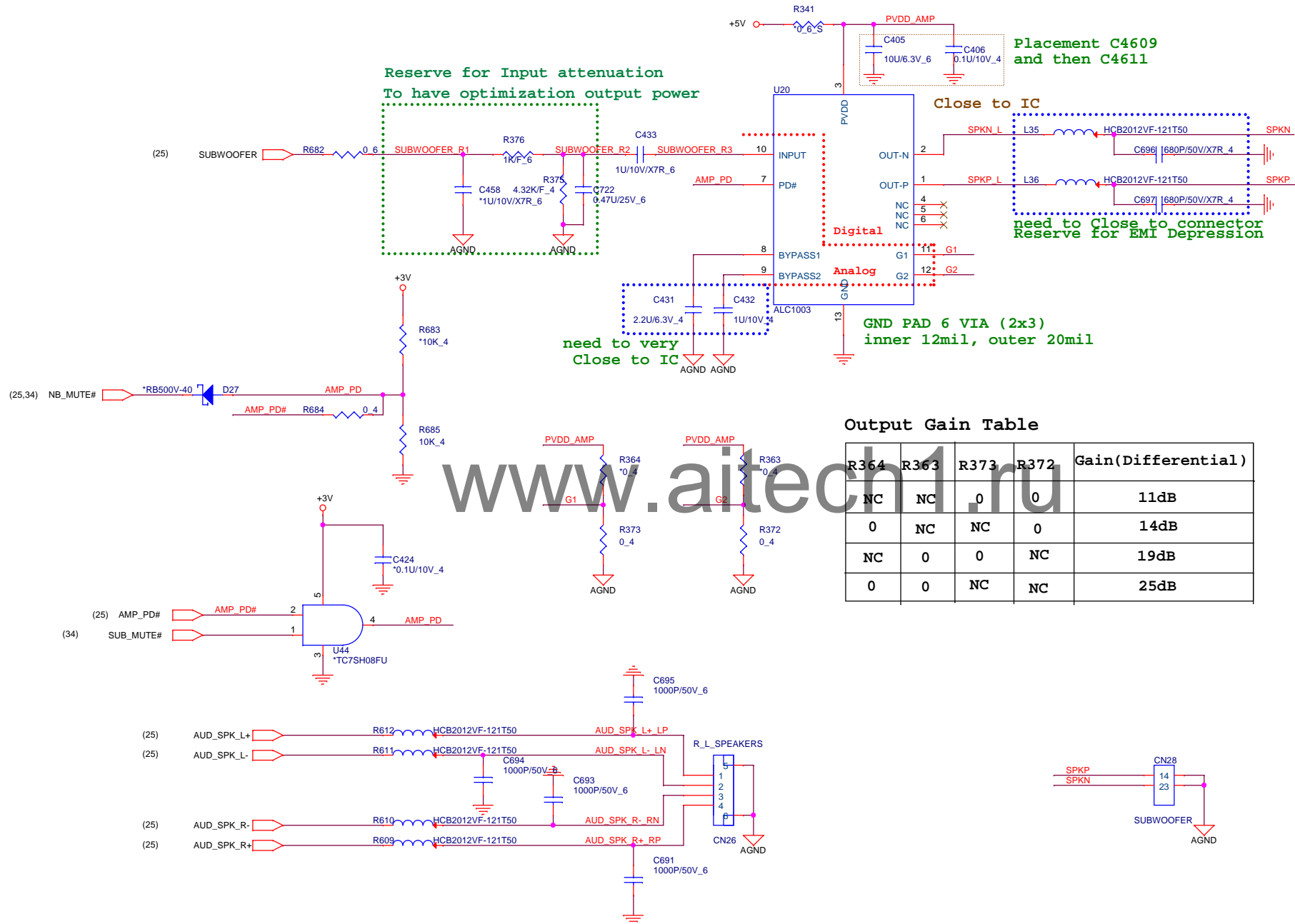
PROJECT : NL8  
Quanta Computer Inc.

Size Document Number  
HDMI CONN  
Date: Friday, April 18, 2014 Sheet 24 of 51 Rev 1A

# ALC283







Placement C4609  
and then C4611

Close to IC

need to Close to connector  
Reserve for EMI Depression

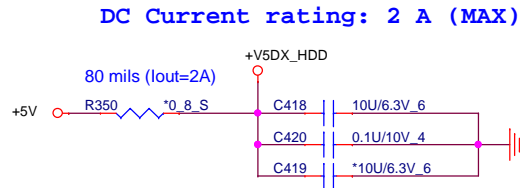
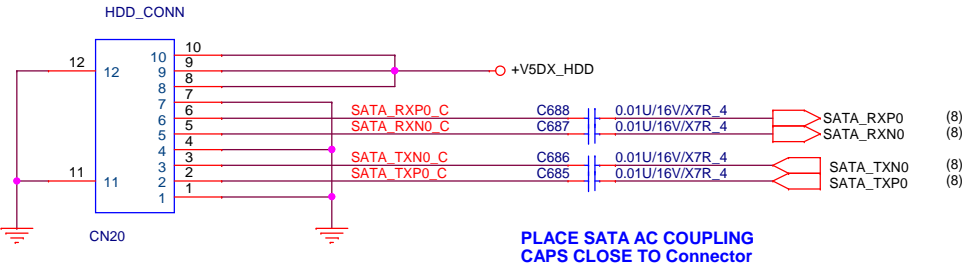
need to very  
Close to IC

GND PAD 6 VIA (2x3)  
inner 12mil, outer 20mil

Output Gain Table

R364	R363	R373	R372	Gain(Differential)
NC	NC	0	0	11dB
0	NC	NC	0	14dB
NC	0	0	NC	19dB
0	0	NC	NC	25dB





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**+3.3V\_ NGFF\_WWAN**  
**Max Current : 2750mA**



**+3.3V\_ NGFF\_WWAN**  
**Max Current : 2750mA**

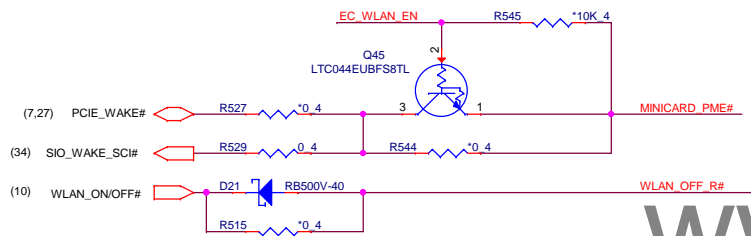
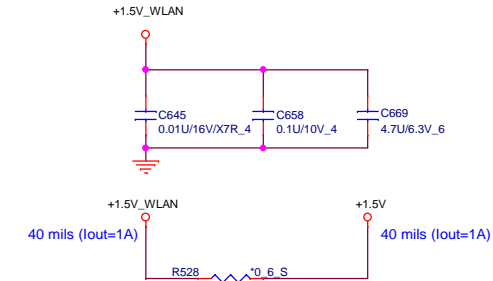
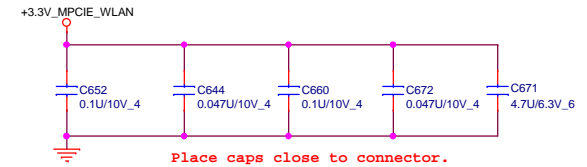
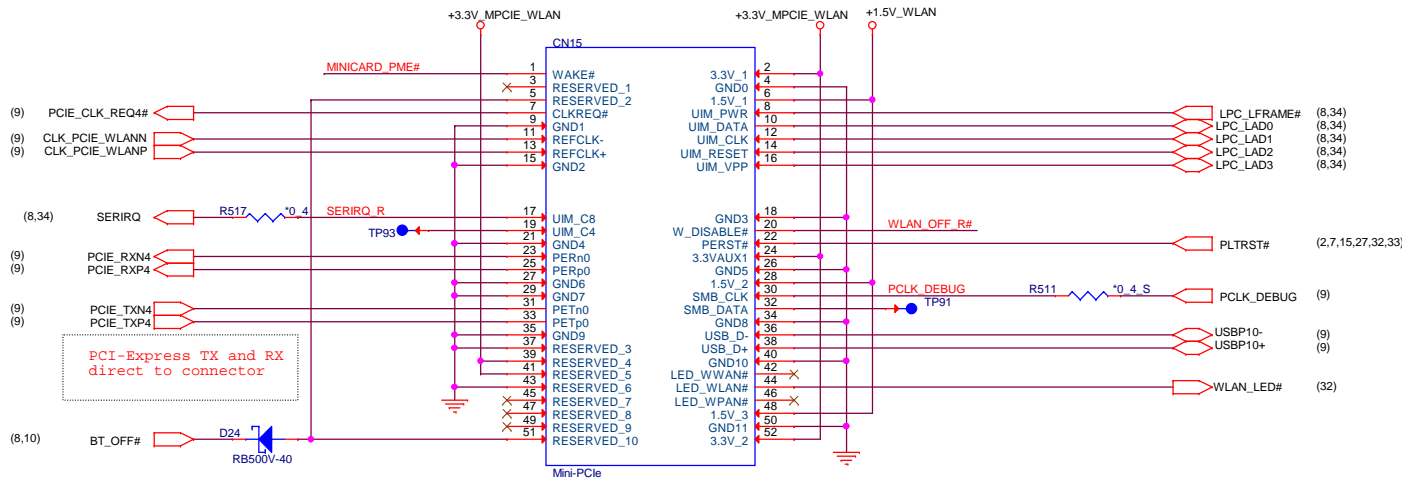


# Mini PCIe Wifi/BT connector

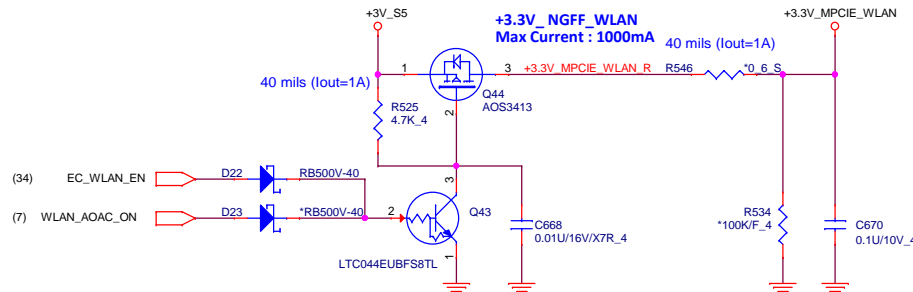
(2,7,8,9,10,11,13,14,15,19,22,23,24,25,26,27,29,32,33,34,35,37,44,45,47)

+3V

30



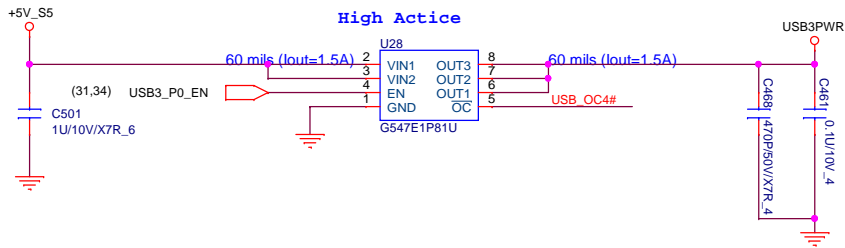
www.aitech1.ru



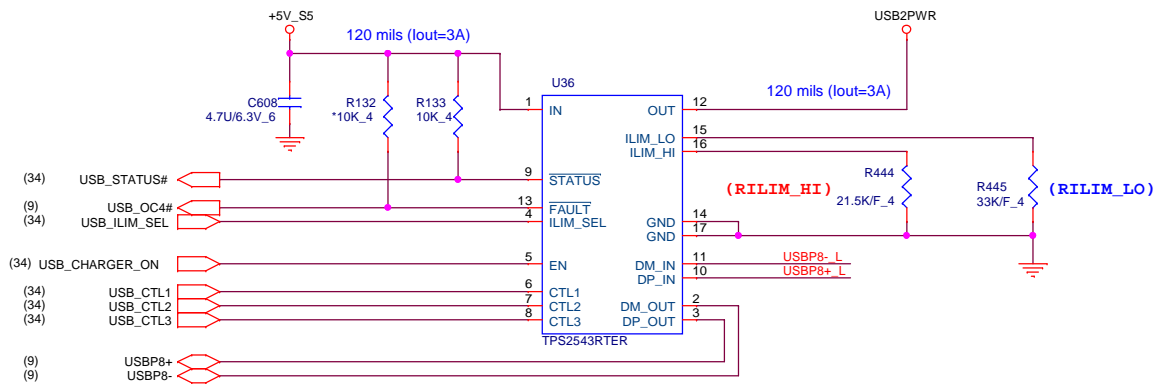
		PROJECT : NL8	
		Quanta Computer Inc.	
Size	Document Number	Wifi/BT MiniPCIE	
Date	Friday, April 18, 2014	Sheet	30 of 51



## USB 3.0 Port



## USB Charger 2.0 Port



RILIM\_LO is optional and the ILIM\_LO pin may be left unconnected if the following conditions are met:

1. ILIM\_SEL is always set high
2. Load Detection - Port Power Management is not used
3. Mouse / Keyboard wake function is not used

If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use RILIM\_LO < 800 kΩ.

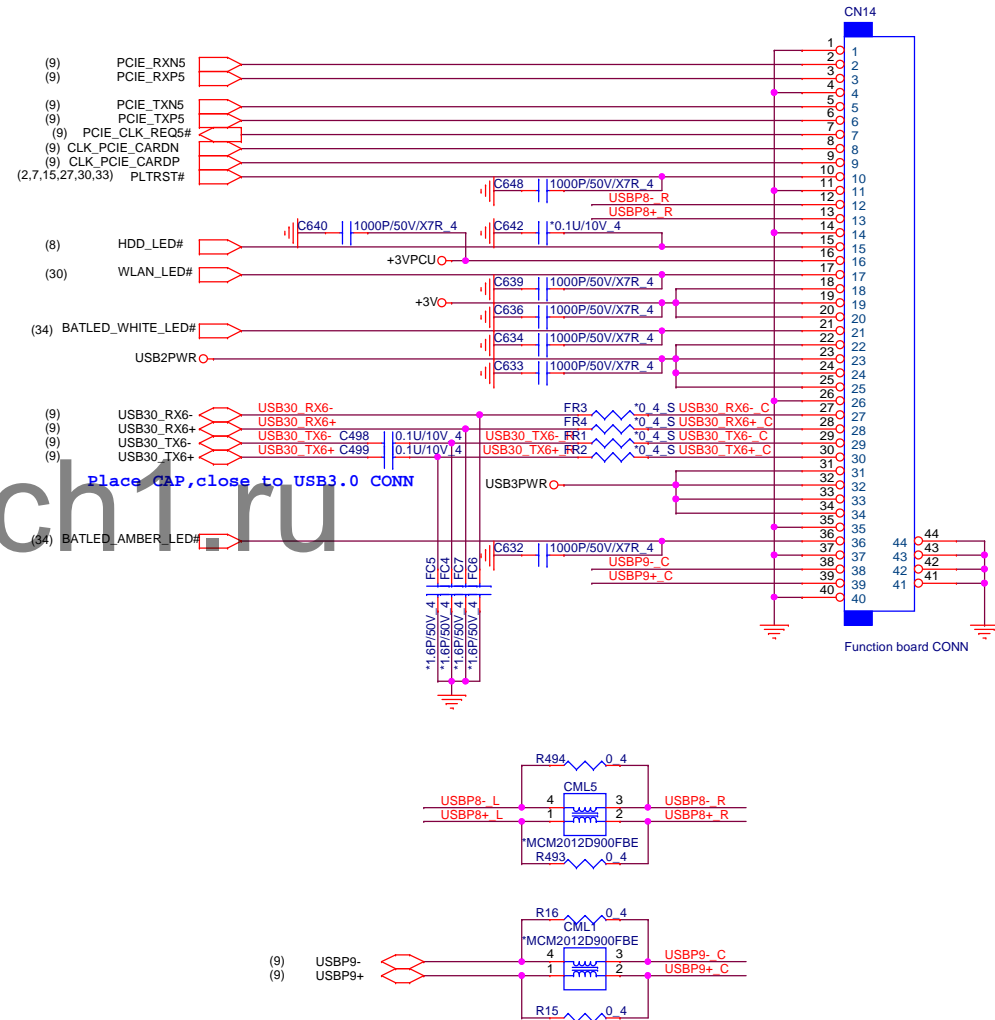
The following equation programs the typical current limit:

$$I_{lim\_xx} \text{ (mA)} = \frac{50,500}{R_{ILIM\_XX} \text{ (}\Omega\text{)}}$$

RILIM\_XX corresponds to either RILIM\_HI or RILIM\_LO as appropriate.

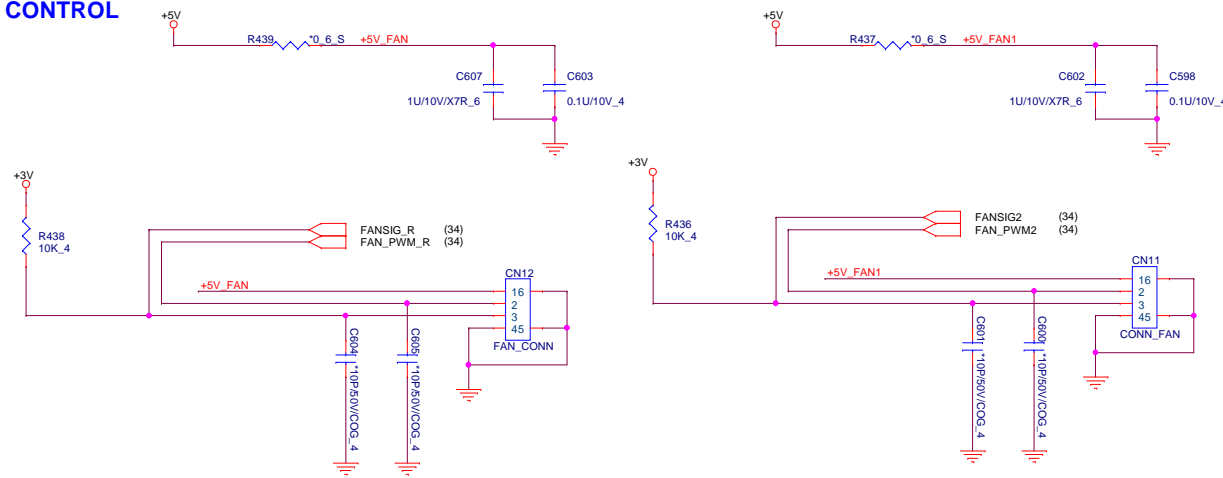
$$I_{OS\_typ}(mA) = \frac{50,500}{(R_{ILIM\_XX}(k\Omega) + 0.1)}$$

## Board to Board

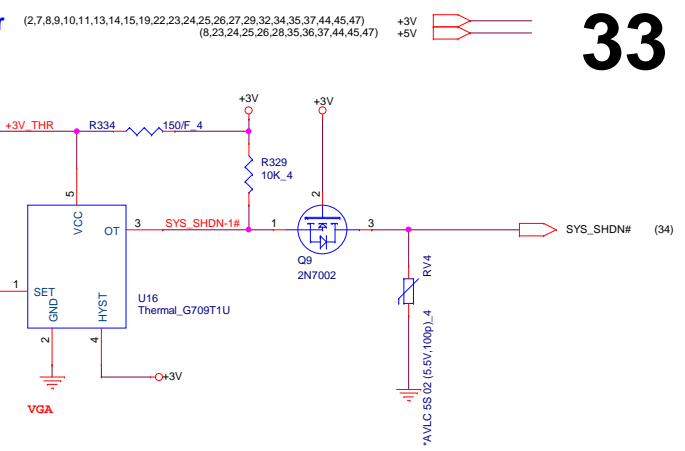




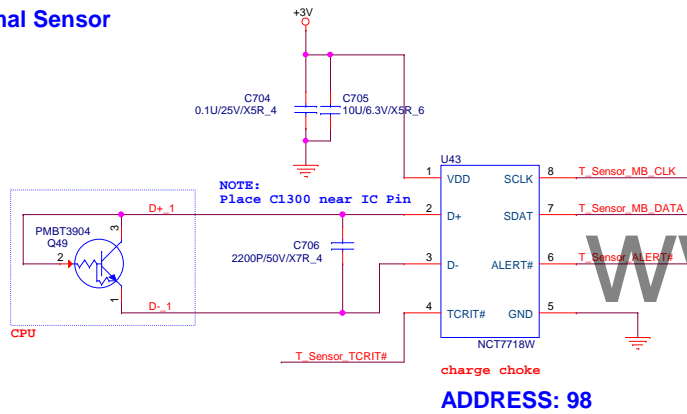
## FAN CONTROL



## Thermal Sensor



## Thermal Sensor



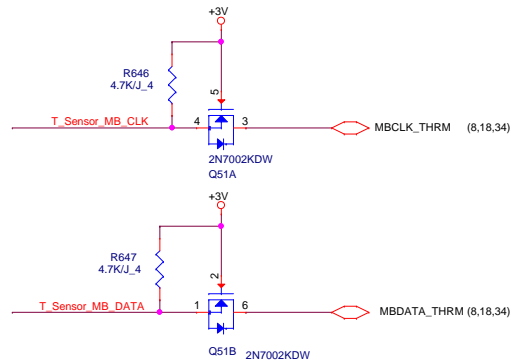
\*Reserved the circuit to isolate the ALERT#/T\_CRIT# pin for power-on T\_CRIT temperature strapping.

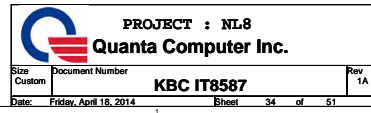
it is to avoid abnormal operation when power on within 100ms for HW strap pin setting HW Shut-down Temp. 109 °C

## ALERT# /T\_CRIT# Pull-up Resistor

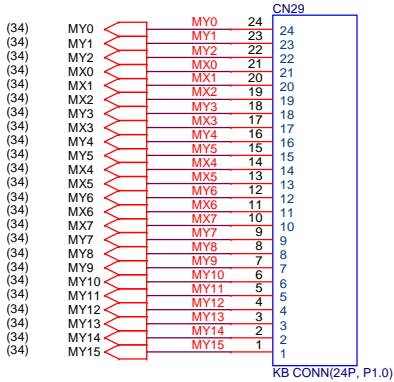
Rb	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77°C	87°C	97°C	107°C	117°C
7.5Kohm	79°C	89°C	99°C	109°C	119°C
10.5Kohm	81°C	91°C	101°C	111°C	121°C
14Kohm	83°C	93°C	103°C	113°C	123°C
18.7Kohm	85°C	95°C	105°C	115°C	125°C

T\_CRIT temperature strapping point





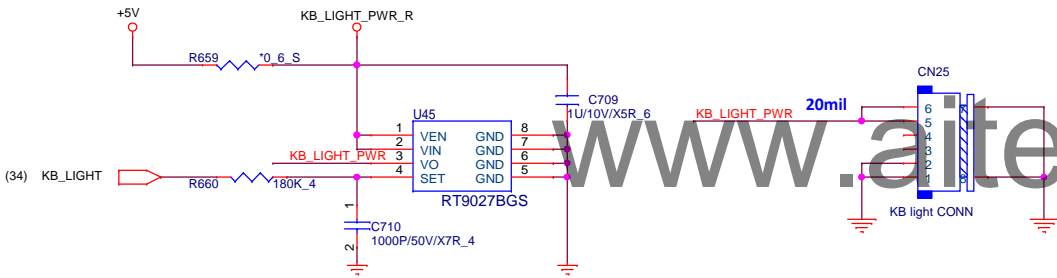
KEYBOARD



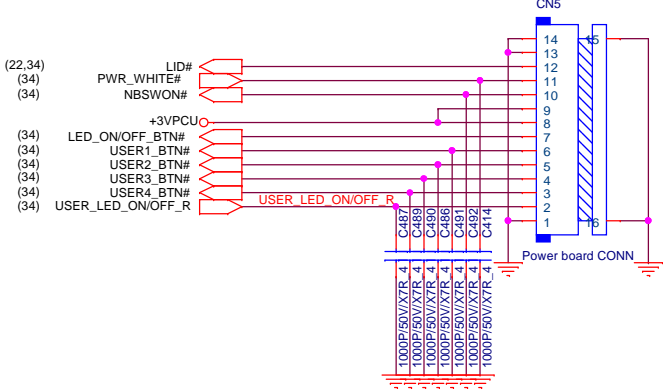
For EMI

MY15	C449	220P/50V/X7R_4	C447	220P/50V/X7R_4	MY13
MY10	C444	220P/50V/X7R_4	C446	220P/50V/X7R_4	MY12
MY11	C445	220P/50V/X7R_4	C456	220P/50V/X7R_4	MY3
MY14	C448	220P/50V/X7R_4	C438	220P/50V/X7R_4	MY6
MX0	C453	220P/50V/X7R_4	C454	220P/50V/X7R_4	MX1
MY1	C451	220P/50V/X7R_4	C440	220P/50V/X7R_4	MX7
MY5	C435	220P/50V/X7R_4	C439	220P/50V/X7R_4	MX6
MX3	C457	220P/50V/X7R_4	C443	220P/50V/X7R_4	MY9
MX2	C455	220P/50V/X7R_4	C442	220P/50V/X7R_4	MY8
MY0	C450	220P/50V/X7R_4	C441	220P/50V/X7R_4	MY7
MX5	C437	220P/50V/X7R_4	C434	220P/50V/X7R_4	MY4
MX4	C436	220P/50V/X7R_4	C452	220P/50V/X7R_4	MY2

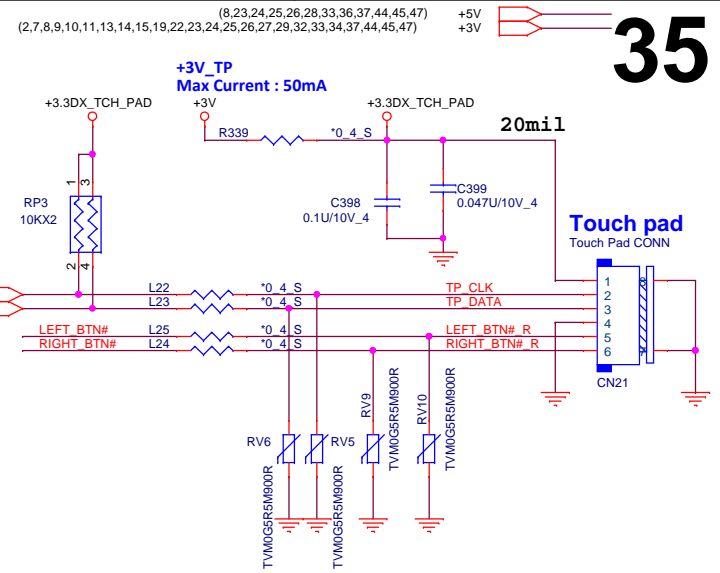
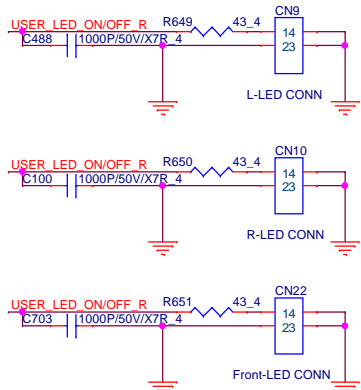
KB Backlit



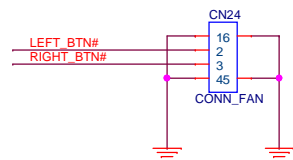
Power board



LED CONN

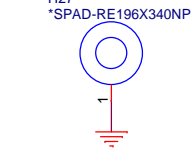
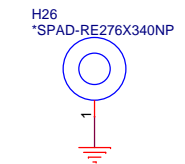
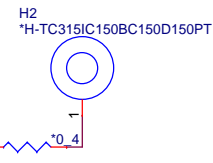
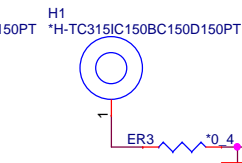
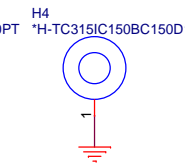
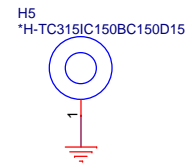
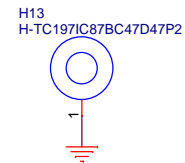
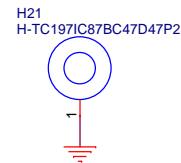
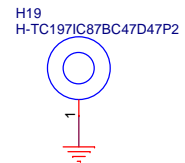
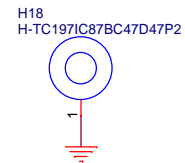
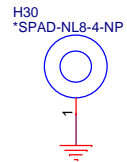
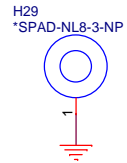
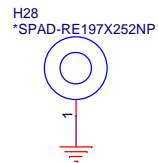
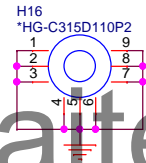
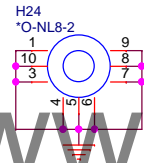
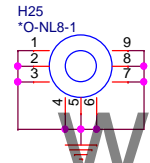
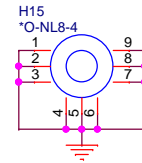
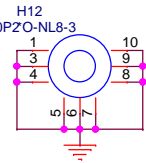
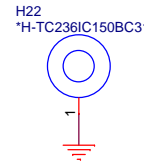
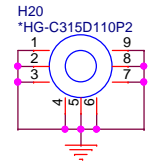
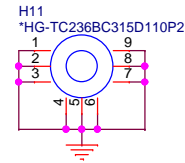
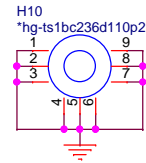
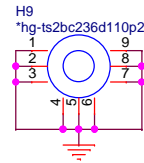
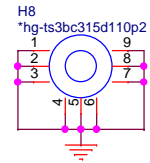
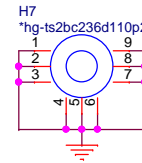
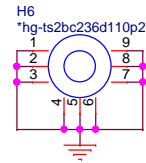
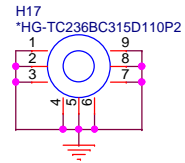
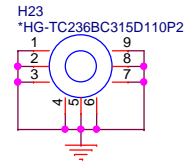
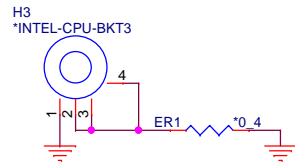


Touch button connector

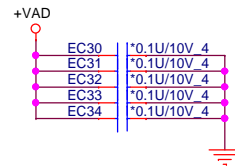
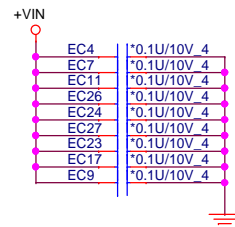
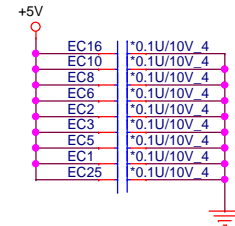


## CPU BRACKET

## INTEL-CPU-BKT3



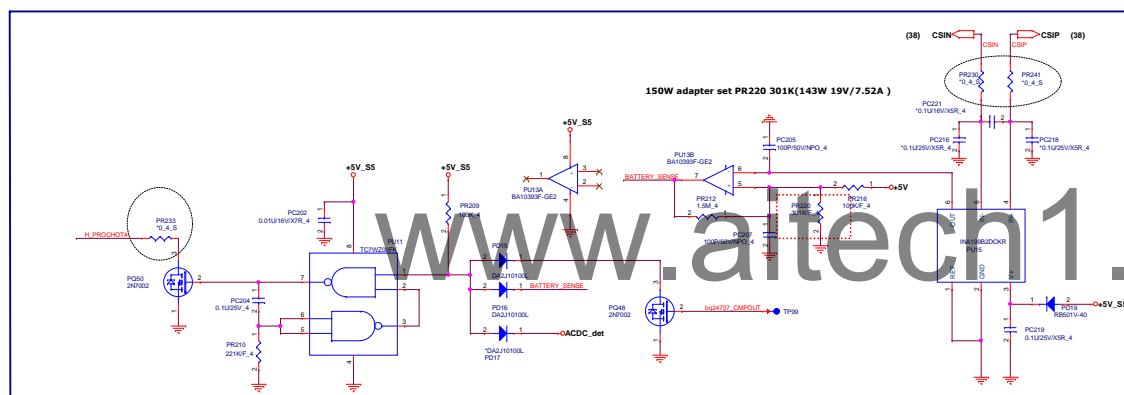
## EMI



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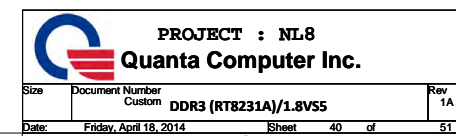
10ms one-shot circuit

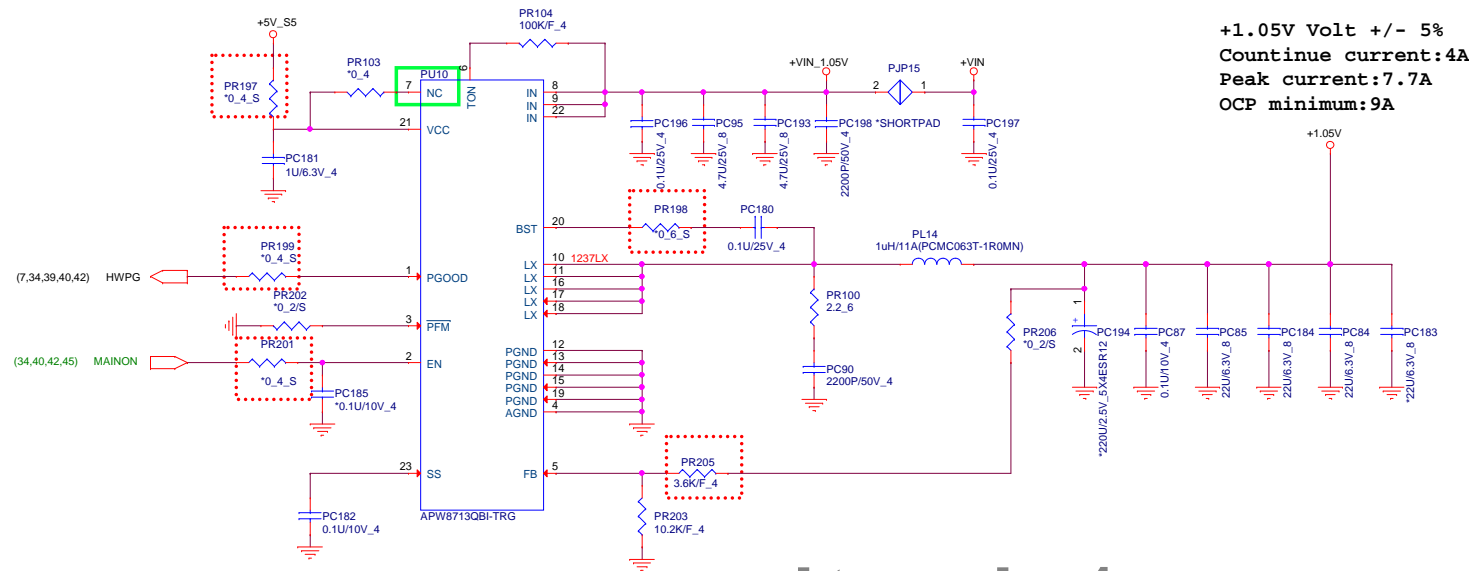




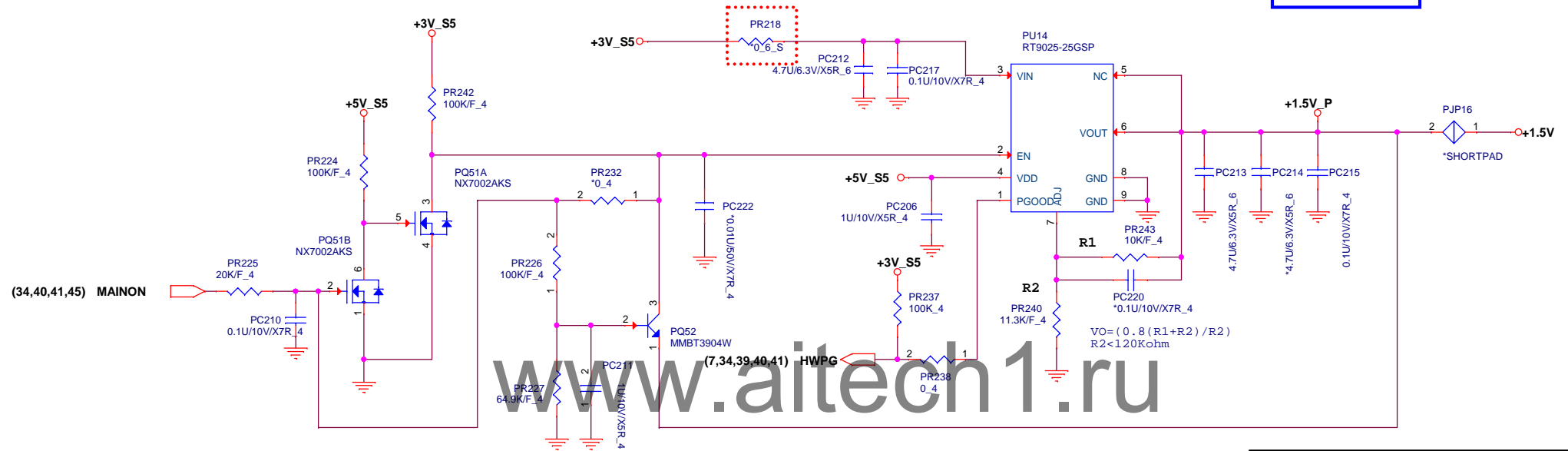




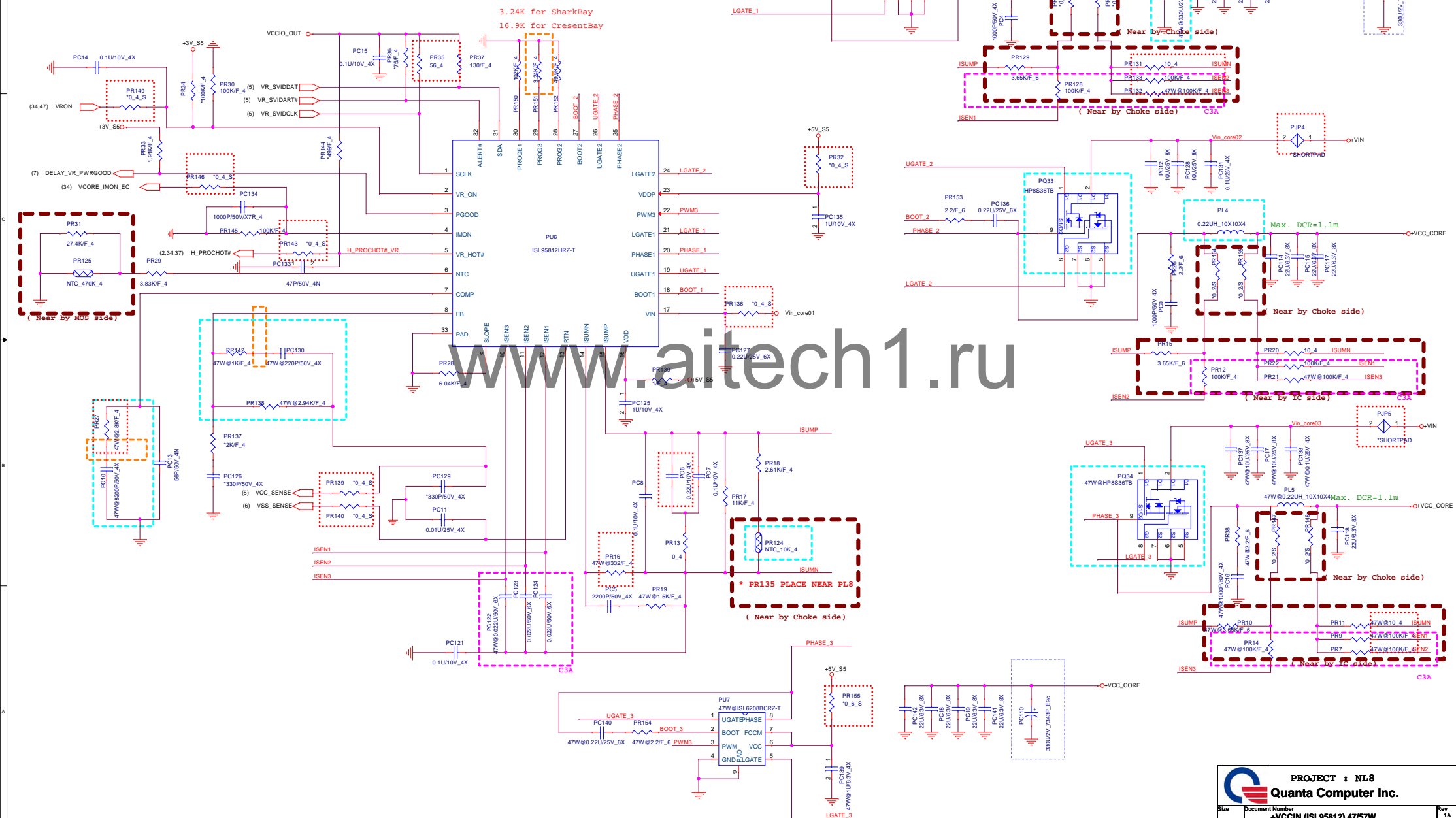


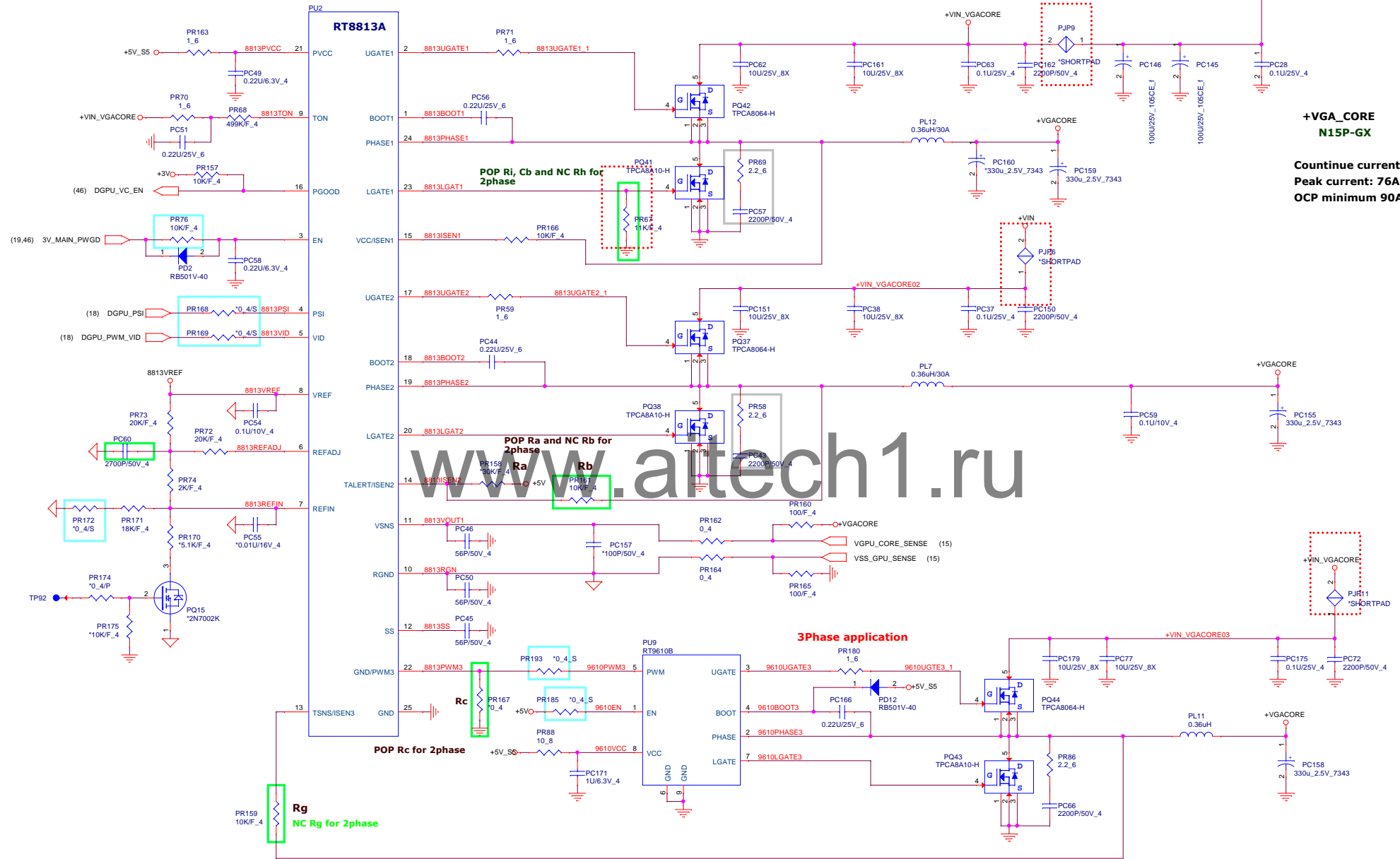


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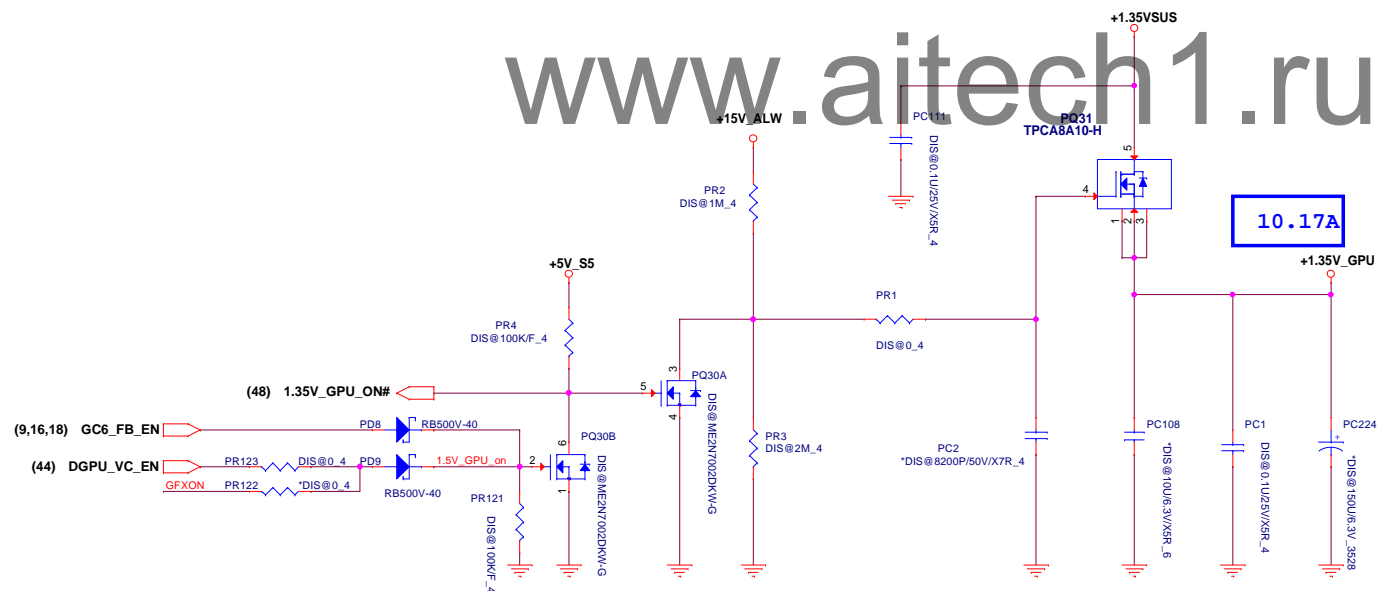
1800



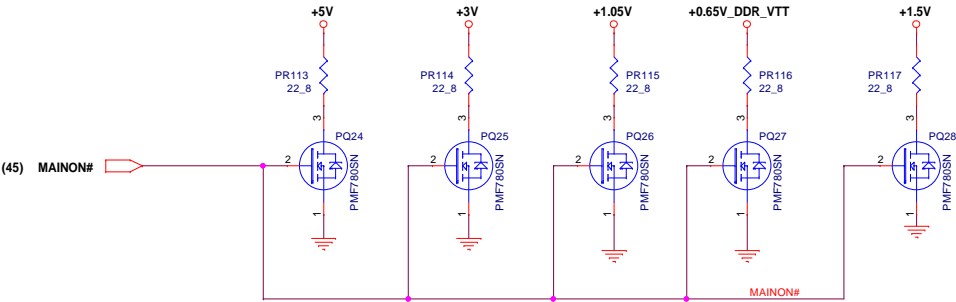




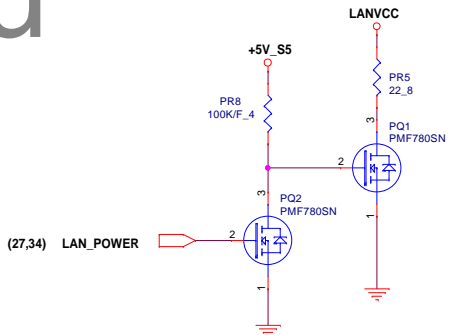
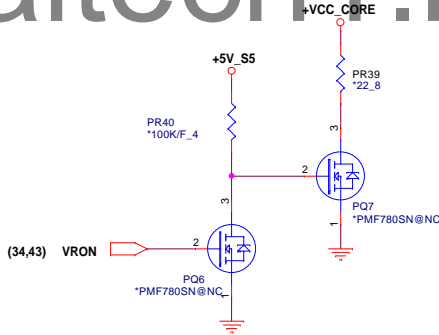
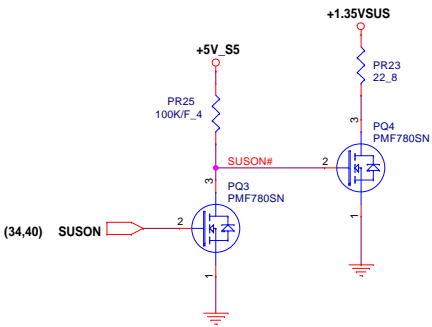
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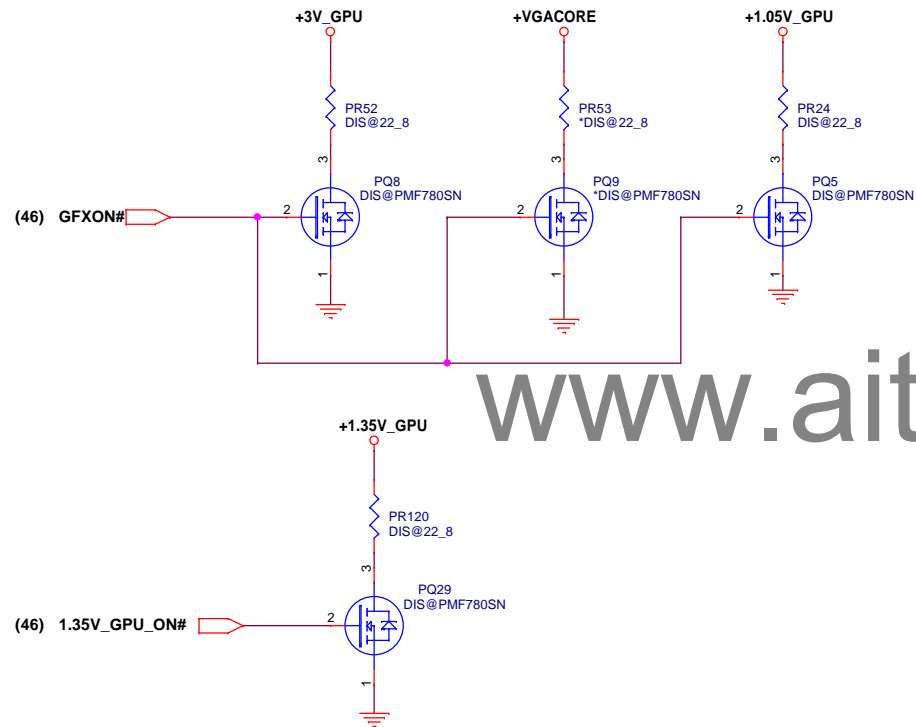




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Discrete only

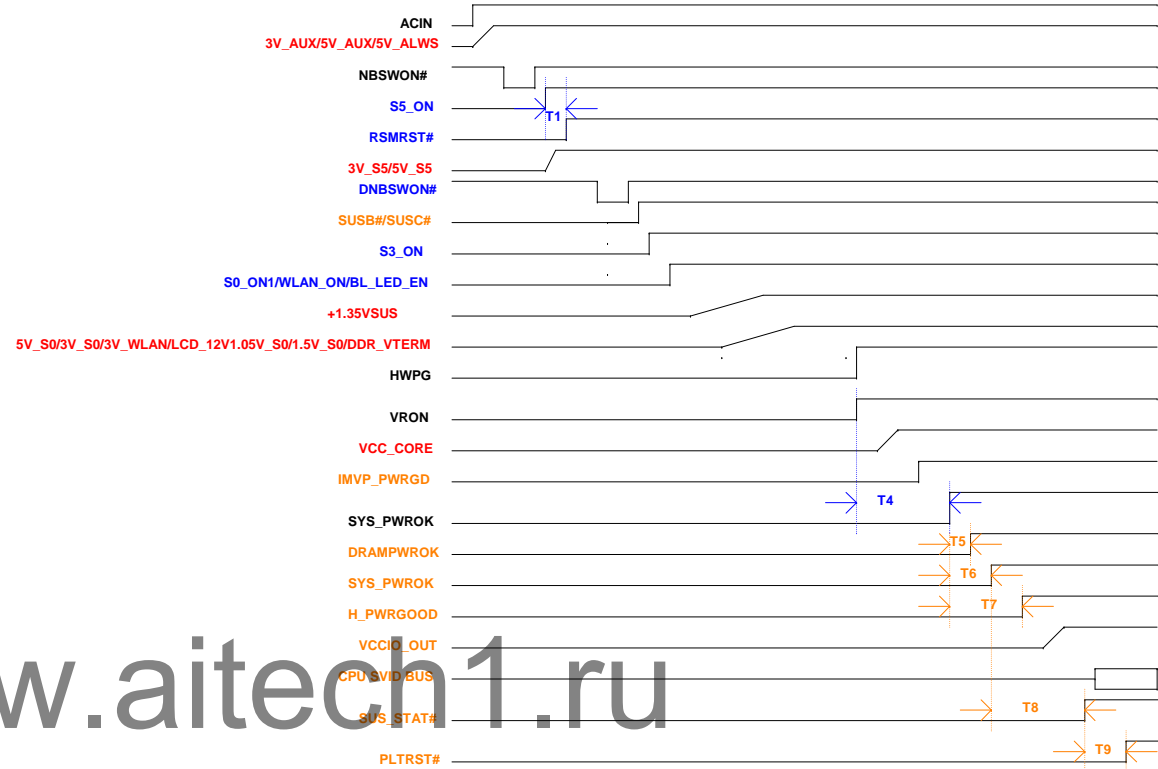


# POWER Sequence Voltage Rails

Power	Voltage	S0	S3	S4	S5	G3	Ctl Signal
3V_RTC	3V	ON	ON	ON	ON	ON	Adaptor in
VIN	19V	ON	ON	ON	ON	OFF	Adaptor in
5V_AUX	5V	ON	ON	ON	ON	OFF	Adaptor in
3V_AUX	3.3V	ON	ON	ON	ON	OFF	Adaptor in
5V_ALWS	3.3V	ON	ON	ON	ON	OFF	3V_AUX
+3V_S5	3V	ON	ON	OFF	OFF	OFF	S5_ON
12V_S5	12V	ON	ON	OFF	OFF	OFF	S5_ON
+1.35VSUS	1.35V	ON	ON	OFF	OFF	OFF	S3_ON
3V_WLAN	3V	ON	OFF	OFF	OFF	OFF	WLAN_ON
LCD_12V	12V	ON	OFF	OFF	OFF	OFF	BL_LED_EN
5V_S0	5V	ON	OFF	OFF	OFF	OFF	S0_ON
+3V	3V	ON	OFF	OFF	OFF	OFF	S0_ON
+1.5V	1.5V	ON	OFF	OFF	OFF	OFF	S0_ON
+1.05V	1.05V	ON	OFF	OFF	OFF	OFF	S0_ON
+0.65V_DDR_VTT	0.675V	ON	OFF	OFF	OFF	OFF	S0_ON
VCC_CORE	By VID	ON	OFF	OFF	OFF	OFF	VRON

## VZ8H SYSTEM POWER-ON SEQUENCE

02



### System Power Sequence

#### EC Control:

T1: S5\_ON TO RSMRST# = 20ms (spec:mini 10ms)

T3: S0\_ON2 TO VRON = 10ms

T4: HWPG TO MPWROK > 5-99ms

Note:HWPG NEED TO BE HIGH at that time

#### System:

T5: MPWROK to DRAMPWROK > 0us(min)

T6: HWPG to SYS\_PWROK =5-99ms

T7: MPWROK to H\_PWRGOOD =2ms(Min)

T8: SYS\_PWROK to SUS\_STAT# =1ms(Min)

T9: SUS\_STAT# to PLTRST# =60us(Min)

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